UNIVERSITI KUALA LUMPUR
Malaysian Institute of Marine Engineering Technology

FINAL EXAMINATION
JANUARY 2016 SESSION

SUBJECT CODE	:	LEB 10403
SUBJECT TITLE	:	DIGITAL ELECTRONICS SYSTEM
LEVEL	:	DEGREE
TIME / DURATION	:	9.00 AM – 12.00 PM / 3 HOURS
DATE	:	18 MAY 2015 / WEDNESDAY

INSTRUCTIONS TO CANDIDATES

1. Please read the instructions given in the question paper CAREFULLY.
2. Begin **EACH** answer on a new page in the Answer Booklet.
3. Where applicable, show clearly steps taken in arriving at the solutions and indicate **ALL** assumptions.
4. This question paper consists of 5 Questions. **Answer Four (4) Questions ONLY.**
5. Tables, Formulae and Charts are appended.
6. Answer all questions in English.

THERE ARE THIRTEEN (13) PAGES OF QUESTIONS, EXCLUDING THIS PAGE.

INSTRUCTION: Answer only FOUR (4) questions.

Please use the answer booklet provided.

Question 1

a. Convert the following binary numbers to their decimal equivalents. Then, perform the addition operation of the binary numbers.

i. 0111 0001 0001

ii. 0010 1100 0110

(4 marks)

b. Analyse the digital numbers given to their respective operation.

i. 011001110 – 000110111

ii. 1001 ÷ 11

(4 marks)

c. As a Digital Circuit Engineer, you are required to come out with an efficient design of digital-to-analogue (DAC) converter circuit in order to rectify the sudden failure electrical system. Apart of your job scope, it demands to analyse the logic circuit as shown in Figure 1. Based on the Figure 1, determine the respective parameters required.

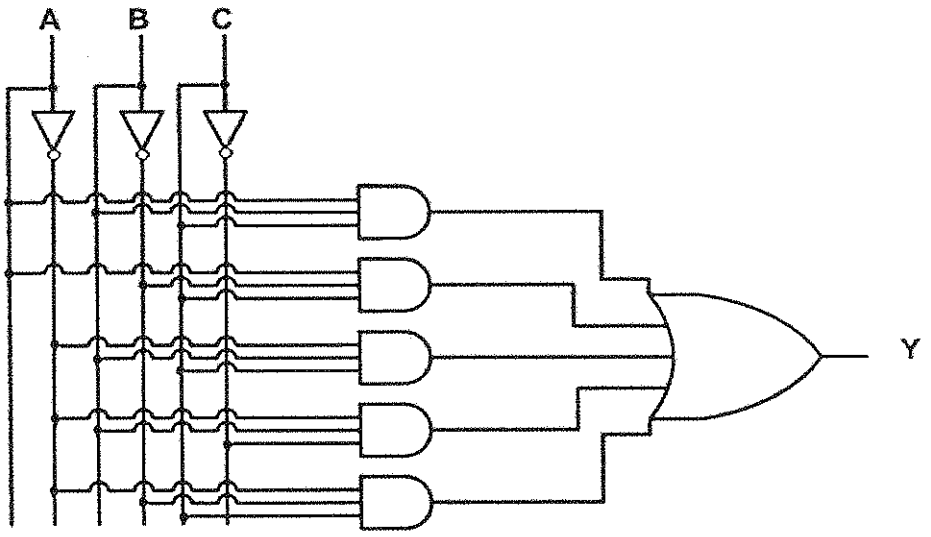


Figure 1

i. Develop the truth table for the logic circuit shown in Figure 1.

(8 marks)

ii. By using Karnaugh Map (K-Map) method, determine the simplified output system, Y.

(4 marks)

iii. Sketch the simplified logic circuit based on your answer in part (ii).

(3 marks)

d. Describes the difference between NOR and NAND gate.

(2 marks)

Question 2

a. Simplify the following Boolean expressions using Boolean and De Morgan Theorems.

i. $Z = \overline{(X+Y)}\left(\overline{Y}+Y\right)$ (2 marks)

ii. $\overline{\overline{(A+B)}+\overline{C}}$ (2 marks)

iii. $T = \overline{\overline{PQR}+(S\overline{Q})+\overline{RQ}}$ (3 marks)

b. For the given function $M(x,y,z) = (\overline{x}\overline{y}\overline{z} + \overline{x}yz + x\overline{yz} + \overline{x}\overline{yz} + xyz)$,

i. Construct the truth table

(4 marks)

ii. Simplify the above function using Karnaugh Map method

(4 marks)

iii. Implement the simplified function in part (b) ii using logic gates.

(3 marks)

c. You're required to design a vending machine that has four different flavors chewing gum; strawberry, grapes, lemon and melon. The chewing gum' prices are stated below:

Flavor	Price (RM)
Strawberry	0.50
Grapes	0.60
Lemon	1.10
Melon	1.50

The vending machine will deliver a package of chewing gum only after pay the exact value for the chewing gum wanted. You may pay through a single coin slot provided that accepts **RM1.00 (O), RM0.50 (F)** or **RM 0.10 (T).** However, you must press the pushbutton before inserting the coins.

The pushbutton is in idle status (B=0) unless you press it (B=1). Design a vending machine that causes Grapes and Lemon flavor of chewing gum to be released to the

customer (B=1). Otherwise, assume B=0. The design of vending machine is expected to have a truth table, logic simplification using K-map method and final logic circuit after simplification.

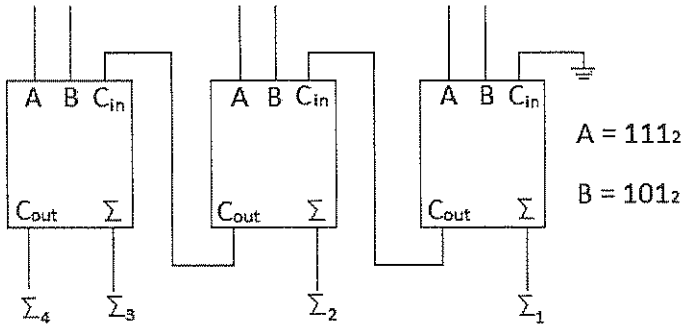
The variables used are summarized as follows:

O F T	B
INPUT	OUTPUT

(7 marks)

Question 3

a. Based on Figure 2, determine the complete sum, ∑ and intermediate carries, C_{out} by analyzing the operation of the circuit in Figure 2.



Figure

(5 marks)

b. Block diagram in Figure 4 shows the full adder where it has 3 inputs, X, Y and carry in (C_{in}). Full adder produces two outputs which are sum, S and carry out (C_{out}).

i. Design a full adder using logic gates

(4 marks)

ii. Show how to implement full adder by using two half adder

(4 marks)

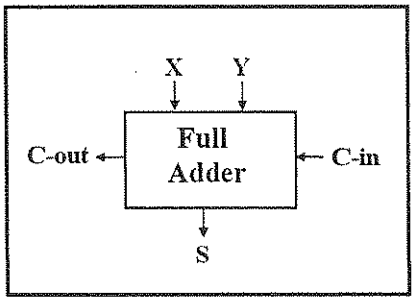


Figure 2

c. Figure 3 shows a block diagram for 2 bit comparator which functions to compare two numbers (A and B) and produces one output, F (A>B). Output F will give logic '1' when the value of A greater than B. Design the 2-bit comparator based on given block diagram.

(4 marks)

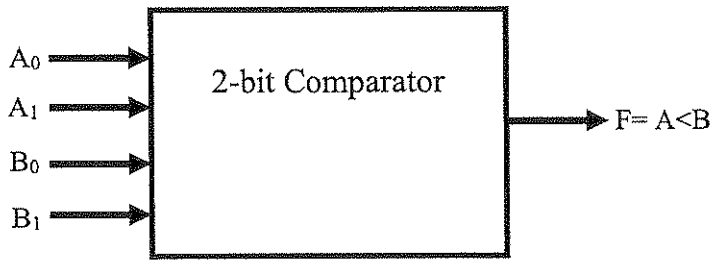


Figure 3

d. Explain the functionality of encoder, decoder, comparator and multiplexer

(8 marks)

Question 4

a. State the difference between latch and flip flop. Describe the functionality of clock in the sequential digital circuit.

(5 marks)

b. J-K flip-flop and S-R latch are two storage elements that are used in building clocked sequential circuits. Create the respective truth table for both types.

(8 marks)

c. Given the waveform shown in Figure 4 are applied to an Active-LOW input S-R latch, draw the resulting Q and $\overline{Q}$ waveform in relation to the inputs. Assume Q starts LOW. (Use Appendix I to draw the output).

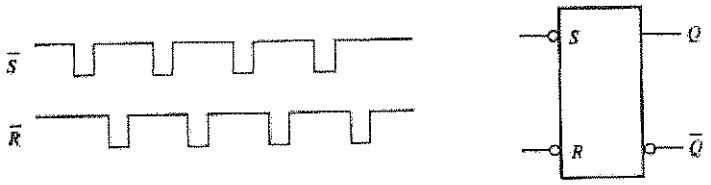


Figure 4

(6 marks)

d. Determine the Q and $\overline{Q}$ output waveform for the gated D latch when given as Figure 5 below. (Use Appendix II to draw the output).

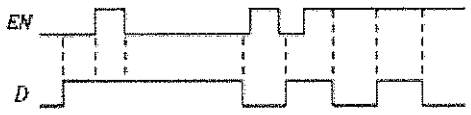


Figure 5

(6 marks)

Question 5

a. Determine the Q and $\overline{Q}$ output waveforms for the inputs given in Figure 6 when the S and R inputs are applied to the gated S-R latch. Show them in proper relation to the enable input. Assume that Q is initially LOW. Start at second pulse of enable input (Use Appendix III to draw the output).

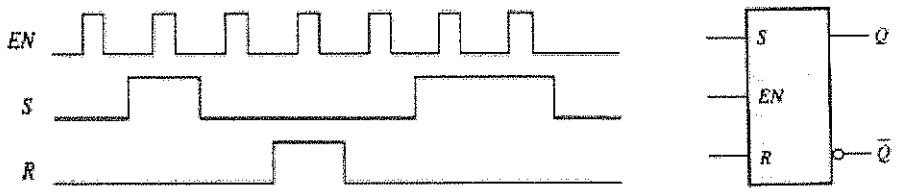


Figure 6 (5 marks)

b. Figure 7 shows a counter with the irregular binary count sequence shown in the state diagram. Use positive edge-triggered J-K flip-flops to design a counter.

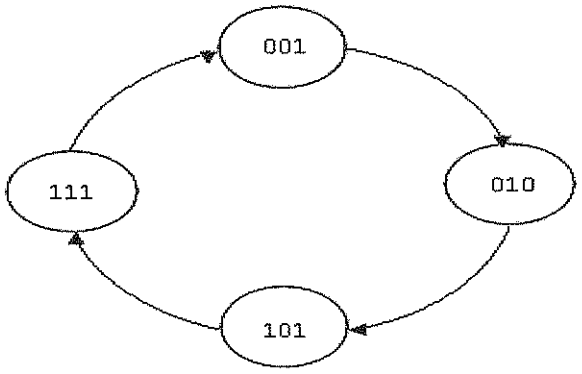


Figure 7

i. Develop a transition state table which consists of present state and next state table. (3 marks)

ii. Develop transition table for J-K flip flop (3 marks)

iii. Simplify the expressions using Karnaugh map. (5 marks)

iv. Construct the circuit design based on the **part b(ii)** obtained. (4 marks)

c. A register is a digital circuit with two basic functions, data storage and data movement. Sketch **two (2)** types of basic data movement in shift registers and rename it respectively.

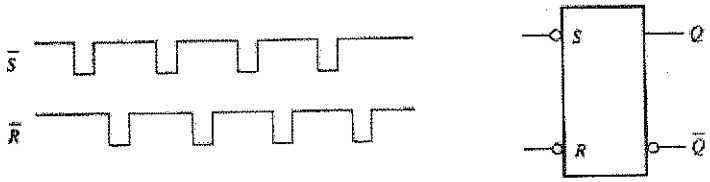
(2 marks)

d. Shift registers are found in many types of applications. Briefly state its application in current technology.

(3 marks)

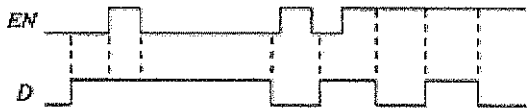
APPENDIX I

Question 4 (c)



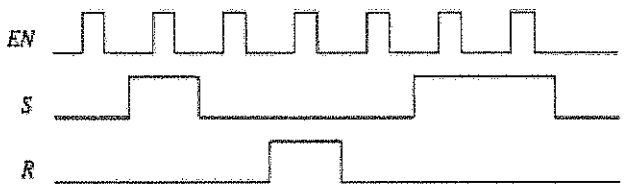
APPENDIX II

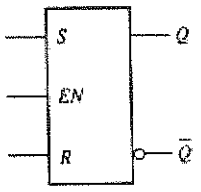
Question 4 (d)



APPENDIX III

Question 5 (a)





END OF QUESTION