UNIVERSITI KUALA LUMPUR
KAMPUS CAWANGAN MALAYSIAN SPANISH INSTITUTE

FINAL EXAMINATION
OCTOBER 2025 SEMESTER

SUBJECT CODE	:	**SAB24603**
SUBJECT TITLE	:	**APPLIED DIGITAL ELECTRONICS**
LEVEL	:	**BACHELOR**
DATE	:	**31 JANUARY 2026**
TIME	:	**02:00PM – 04:30PM**
DURATION	:	**2 HOURS 30 MINIUTES**

INSTRUCTIONS TO CANDIDATES

1. Please read the instructions given in the question paper CAREFULLY.
2. This question paper consists of **SIX (6)** Questions.
3. Answer **ALL** Questions in **Section A**. Answer **ONLY THREE (3) OUT OF FOUR (4)** Questions in **Section B** in the answer booklet provided.
4. Where applicable, show clearly steps taken in arriving at the solutions and indicate ALL assumptions.
5. Answer ALL questions in English language only.

THERE ARE 5 PAGES OF QUESTIONS, EXCLUDING THIS PAGE.

SECTION A (Total: 40 marks)

INSTRUCTION: Answer ALL questions in Section A.
Please use the answer booklet provided.

Question 1

a) Sketch logic gates for full-adder circuit.

(5 marks)

b) Solve expression shown by applying De Morgan's theorem

$$X = \overline{\overline{A}B + A\overline{B}}$$

(7 marks)

c) Simplify using Karnaugh map for below expression.

$$X = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + A\overline{B}\overline{C} + A\overline{B}C$$

(3 marks)

d) A 7-segment display LED in Figure 2 is able to display from 0 until 9. Write a Verilog code represented **"F"** output respectively.

(5 marks)

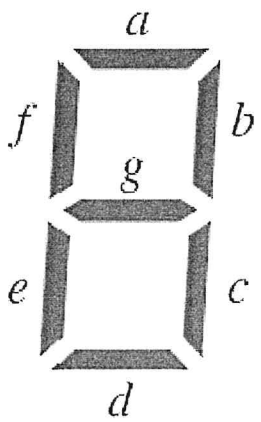

Figure 2

Question 2

Write the full Verilog behavioral AND structural description code for the circuits schematic as shown in Figure 3 and Figure 4.

a)

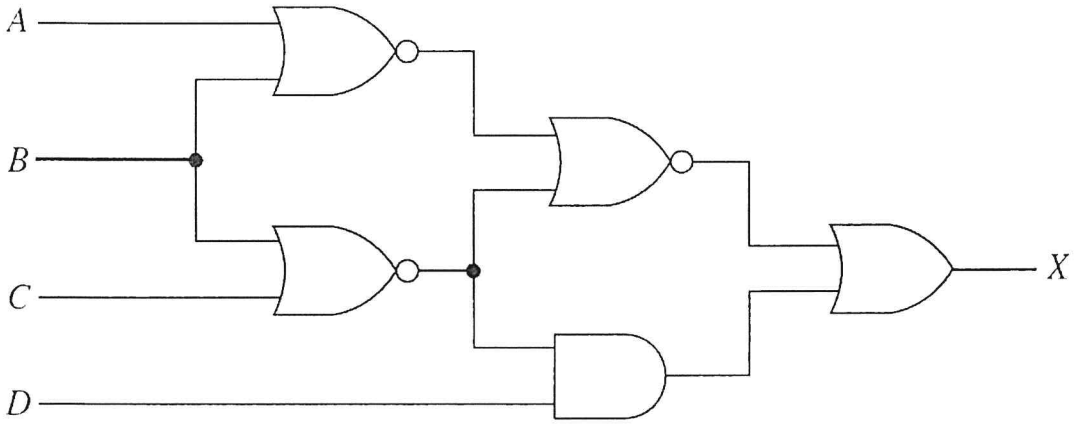

Figure 3

(10 marks)

b)

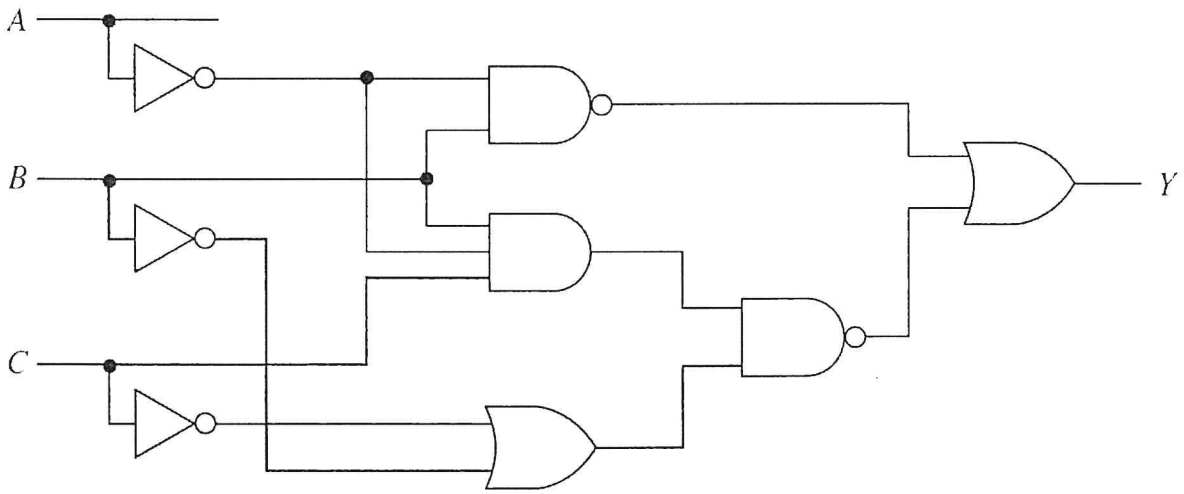

Figure 4

(10 marks)

SECTION B (Total: 60 marks)

INSTRUCTION: Answer 3 out of 4 questions in Section B.

Question 3

a) Draw the logic circuit schematic for the Verilog behavioral description codes below.

i.
```
module Q1a(A,B,C,D,E,X);
input A,B,C,D,E;
output X;
wire G1,G2,G3,G4,G5;

    or(G3,~A,~B,~(~C));
    or(G5,~(~C),~D);
    nand(G2,G3,E);
    nand(G4,E,G5);
    or(G1,~G2,~G4);
    buf(X,G1);

endmodule
```

(8 marks)

ii.
```
module Q1b(A1,A2,B1,B2,X);
input A1,A2,B1,B2;
output X;
wire G1,G2,G3,G4,G5,G6,G7;

    not(G6,B1);
    not(G7,B2);
    and(G1,A1,A2);
    and(G2,A2,G6);
    and(G3,G6,G7);
    and(G4,G7,A1);
    or(G5,G1,G2,G3,G4);
    buf(X,G4);

endmodule
```

(8 marks)

b) Write Verilog code which apply **if-else** statement corresponding to the logic circuit shown in Figure 5 below.

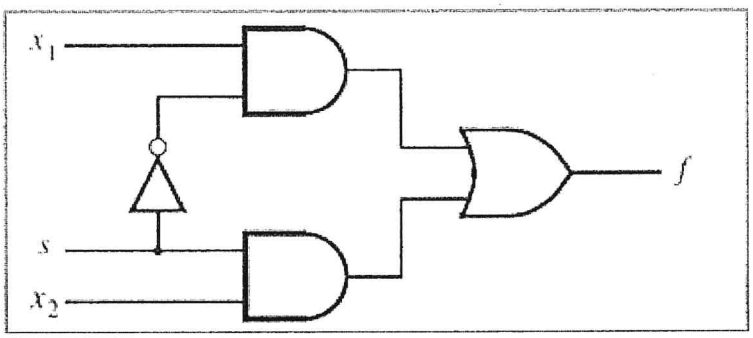

Figure 5

(4 marks)

Question 4

a) Construct the circuit based on the Verilog code given below.

```
module example2 (x1, x2, x3, x4, f, g, h);
    input x1, x2, x3, x4;
    output f, g, h;

    and (z1, x1, x3);
    and (z2, x2, x4);
    or (g, z1, z2);
    or (z3, x1, ~x3);
    or (z4, ~x2, x4);
    and (h, z3, z4);
    or (f, g, h);

endmodule
```

(5 marks)

b) Design a modulus-8 synchronous counter that will count down 8 numbers which starts from 7_{10} (111_2) to 0_{10} (000_2) and count back to 7_{10} (111_2). Use positive edge-triggered D flip flops.

(15 marks)

Question 5

a) State the difference between latch and flip-flop. Provide THREE (3) types of latches and flip-flops respectively.

(6 marks)

b) Sketch the diagram and show the truth table for edge-triggered J-K flip flop.

(10 marks)

c) Write a Verilog code for **D flip flop** during a positive edge triggered condition.

(4 marks)

Question 6

a) Provide differentiation between encoder and decoder

(6 marks)

b) Draw a graphical symbol for 2-to1 multiplexer and its truth table.
Assume: ω_0 and ω_1 as an input of multiplex

(6 marks)

c) Write a Verilog code of multiplexer 4-to-1 input output

(8 marks)

END OF EXAMINATION PAPER