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CONFIDENTIAL

SET A

UNIVERSITI KUALA LUMPUR
Malaysia France Institute

FINAL EXAMINATION

JANUARY 2014 SESSION

SUBJECT CODE	:	**FLB 23033**
SUBJECT TITLE	:	**DIGITAL SYSTEM**
LEVEL	:	**BACHELOR**
TIME / DURATION	:	**3.0 HOURS**
DATE	:	

INSTRUCTIONS TO CANDIDATES

1. **Please read the instructions given in the question paper CAREFULLY.**
2. **This question paper is printed on both sides of the paper.**
3. **Please write your answers on the answer booklet provided.**
4. **Answers should be written in blue or black ink except for sketching, graphic and illustration.**
5. **This question paper consists of TWO (2) sections. Section A and B. Answer all questions in Section A. For Section B, answer two (2) questions only.**
6. **Answer all questions in English.**

THERE ARE 6 PAGES OF QUESTIONS, EXCLUDING THIS PAGE AND APPENDIX.

SECTION A (Total: 60 marks)

INSTRUCTION: Answer ALL questions.

Please use the answer booklet provided.

Question 1

(a) Assuming that all numbers are **16 bit wide**, complete the missing entries which are not shaded in the **Table 1**.
(Fill-up the answer in Appendix 1 and submit the page with your answer booklet).

Table 1

Decimal	Binary	Octal	Hexadecimal	Gray Code
			BAE	
				1100 0100 1100
		68		
			19A	
	1000 0111 0111			
37.375				

(8 marks)

(b) Using 8-bit 2's complement arithmetic, perform the following arithmetic operations where $M = 56_8$ and $N = 6B_{16}$. Verify your answers with decimals values. Indicate if invalidity exists.

i. $M + N$

ii. $M - N$ (6 marks)

(c) Perform addition of the following decimal numbers in BCD system. Verify your answers with decimals.

i. $45_{10} + 16_{10}$

ii. $29_{10} + 69_{10}$ (6 marks)

Question 2

(a) **Figure 1** shows a combinational logic circuit with three inputs *a, b* and *c,* and an output, *H.*

i. Obtain the output expression for $H(a, b, c)$.

ii. Simplify the expression using Boolean algebra and/or De Morgan theorem

iii. Draw the simplified circuit.

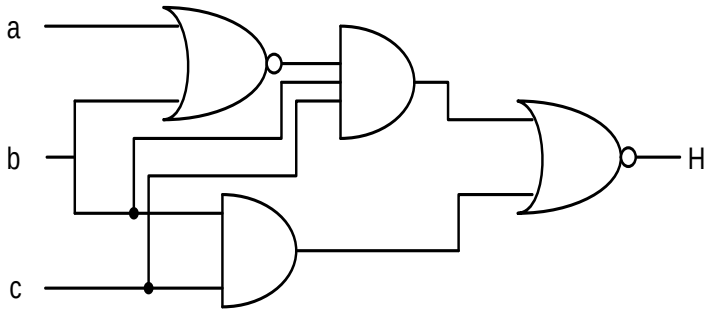

Figure 1

(10 marks)

(b) Simplify the following Boolean expressions using Boolean algebra and/or De Morgan theorem.

$$P = \overline{A}C + \overline{A}\,\overline{C}\,D + ABC + AB\overline{C}\,D$$ (4 marks)

(c) Simplify the following Boolean equation, in sum-of-products form, using Karnaugh map.

$Y(a, b, c, d) = \sum m\ (0,2,4,5,6,8,10)$, with 'don't care' condition at $D(9,12,13,14)$

(6 marks)

Question 3

(a) Consider the Boolean function $f = AB + AC + \bar{A}\bar{B}\bar{C}$

Implement this function using one *4 X 1* multiplexer, with the restriction that the variable *C* cannot be connected to a multiplexer select line.

(10 marks)

(b) For the circuit shown in **Figure 2**, determine the Boolean expressions for the logic functions *P* and *Q*.

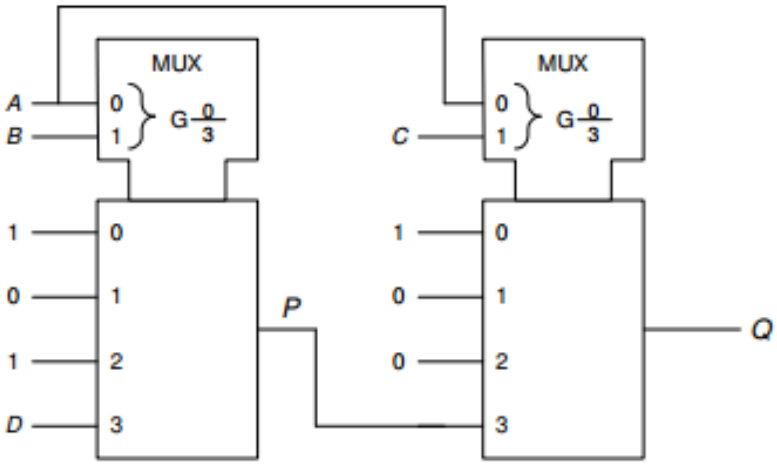

Figure 2

(4 marks)

(c) **Table 2** shows the output transitions for a *J-K* flip-flop. Give the values of the inputs *J* and *K* necessary to obtain these output transitions. Fill-up the answer in Table for Question 3 (c) provided in the Appendix on page 7, and submit the page with your answer booklet.

Table 2

Output transition	J	K	Condition
0 → 0			
0 → 1			
1 → 0			
1 → 1			

(6 marks)

SECTION B (Total: 40 marks)

INSTRUCTION: Answer only TWO (2) questions
Please use the answer booklet provided.

Question 4

(a) **Figure 4** shows a 3-bit synchronous counter using JK flip flop.

i. Derive the input equations for each flip-flop. (3 marks)
ii. Determine the MOD number of the counter. (3 marks)
iii. Draw the state table and state diagram for the circuit (6 marks)

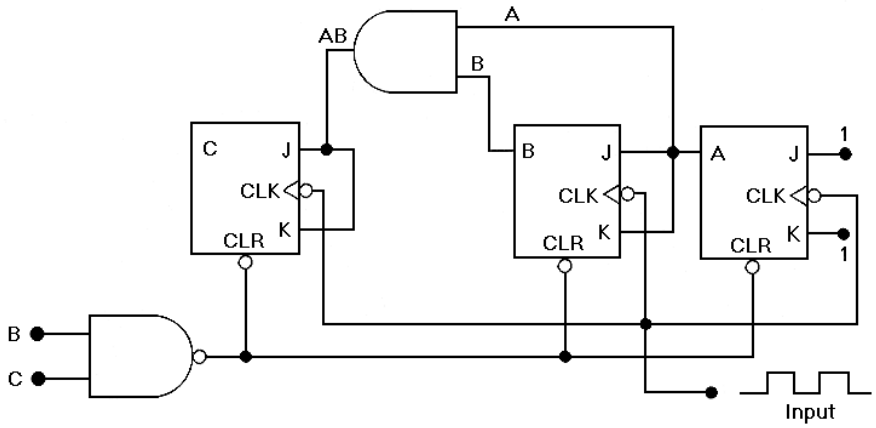

Figure 4

(b) How many FFs are required for the MOD-60 counter? (2 marks)

(c) Construct a MOD-10 counter that will count from 0000 through 1001 (6 marks)

Question 5

A bottling system is shown in **Figure 5**. There are three (3) sensors A, B, and C which detect the filling, capping and the labelling process of the bottles respectively. The procedure are:

- At station 1, if the bottle is empty, sensor A will produce an input one (1) and the drift actuator will feed the tablets into the bottle. Otherwise sensor A will produce a zero (0) input and the bottles continues to the next section
- At station 2, if there is no cap, sensor B will produce and input one (1) and send the signal to the capping actuator to carry out the task. Otherwise, sensor B will produce a zero (0) input and the bottle continues to the next section.
- At station 3, if there is no label, sensor C will produce an input one (1) and send the signal to the labelling actuator to carry out the task. Otherwise, sensor C will produce a zero (0) input and the bottle continues moving.
- The bottle will be rejected:
  - If it has no tablet but has a cap
  - If it has no tablet but has a cap and has a label

(a) Determine the number of input(s) and output(s) this system has. (5 marks)

(b) Derive the truth table for this system (5 marks)

(c) Determine the simplified expression using a Karnaugh map technique for the system output(s). (6 marks)

(d) Draw the simplified circuit (4 marks)

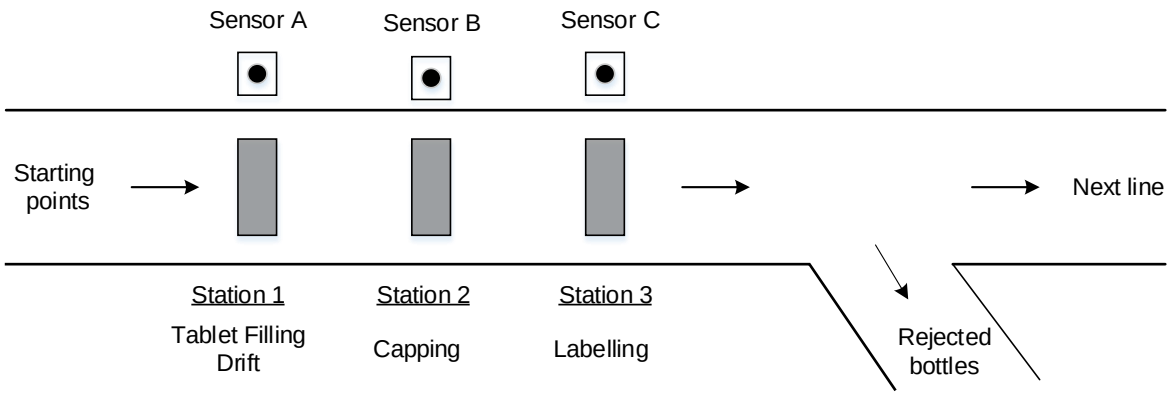

Figure 5

Question 6

(a) Design a 3 x 8 decoder used for Binary to Octal conversion by showing the following steps.

i. Truth Table (4 marks)

ii. Logic circuit (4 marks)

iii. Output expressions (4 marks)

(b) Draw the block diagram of a Full-Adder and its truth table, and determine its output expressions

(8 marks)

END OF QUESTION PAPER

APPENDIX 1

(SUBMIT WITH ANSWER BOOKLET)

Boolean algebra and De Morgan's theorems

1. $X \bullet 0 = 0$
2. $X \bullet 1 = X$
3. $X \bullet X = X$
4. $X \bullet \overline{X} = 0$
5. $X + 0 = X$
6. $X + 1 = 1$
7. $X + X = X$
8. $X + \overline{X} = 1$
9. $X + Y = Y + X$
10. $X \bullet Y = Y \bullet X$
11. $X + (Y + Z) = (X + Y) + Z = X + Y + Z$
12. $X(YZ) = (XY)Z = XYZ$

13a. $X(Y + Z) = XY + XZ$

13b. $(W + X)(Y + Z) = WY + XY + WZ + XZ$

14. $X + XY = X$
15. $X + \overline{X}Y = X + Y$
16. $\overline{X + Y} = \overline{X}\,\overline{Y}$
17. $\overline{XY} = \overline{X} + \overline{Y}$
18. $\overline{\overline{A}} = A$

Answer Table for Question 1(a)

Decimal	Binary	Octal	Hexadecimal	Gray Code
			BAE	
				1100 0100 1100
		68		
			19A	
	1000 0111 0111			
37.375				

Answer Table for Question 3(c)

Output transition	J	K	Condition
0 → 0			
0 → 1			
1 → 0			
1 → 1			