UNIVERSITI KUALA LUMPUR
KAMPUS CAWANGAN MALAYSIAN SPANISH INSTITUTE

FINAL EXAMINATION
OCTOBER 2025 SEMESTER

COURSE CODE	: SAB 36203
COURSE NAME	: ANALOG IC DESIGN AND VERIFICATION
PROGRAMME LEVEL	: BACHELOR
DATE	: 31 JANUARY 2026
TIME	: 09.00 AM – 11.30 AM
DURATION	: 2 HOURS 30 MINUTES

INSTRUCTIONS TO CANDIDATES

1. Please read the instructions given in the question paper CAREFULLY.
2. This question paper consists of FIVE (5) QUESTIONS.
3. Answer FOUR (4) questions only.
4. Please write the answer in the answer booklet provided.
5. Answer all questions in English language ONLY.

THERE ARE 5 PAGES OF QUESTIONS, EXCLUDING THIS PAGE.

Question 1

Sketch and explain the operating conditions of a **MOS Capacitor** for the following:

(a) $V_G << V_{TN}$

(5 marks)

(b) $V_G < V_{TN}$

(10 marks)

(c) $V_G > V_{TN}$

(10 marks)

Question 2

Consider In the Zener-regulated power supply shown in Figure 1, the input voltage v_I has an RMS value of 15 V, and the operating frequency is 60 Hz. The circuit includes a resistor R=100 Ω, and a capacitor C=1000 μF. The diodes D_1 and D_2 each have an on-voltage of 0.75 V, while the Zener diode D3 has a Zener voltage of 15 V.

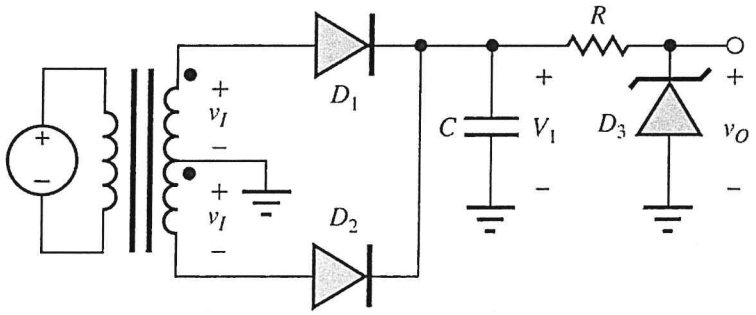

Figure 1: Rectifier circuit.

(a) State the type of rectifier is used in this power supply circuit.

(5 marks)

(b) Determine the dc voltage at V_1.

(5 marks)

(c) Find the dc output voltage v_O.

(5 marks)

(d) Determine the magnitude of the ripple voltage at V_1.

(5 marks)

(e) Find the minimum PIV rating for the rectifier diodes.

(5 marks)

Question 3

A MOSFET common-source amplifier is a basic amplifier configuration where the input signal is applied to the gate, and the output is taken from the drain as shown in Figure 2. Analyze the given common-source amplifier circuit to determine its performance characteristics. Using the provided parameters K_n=0.50 mA/V^2, V_{TN}=1 V, λ=0.0133 V^{-1} and the Q-point (0.241 mA, 3.81 V). Ensure that the transistor remains in the active region and consider small-signal assumptions throughout the analysis.

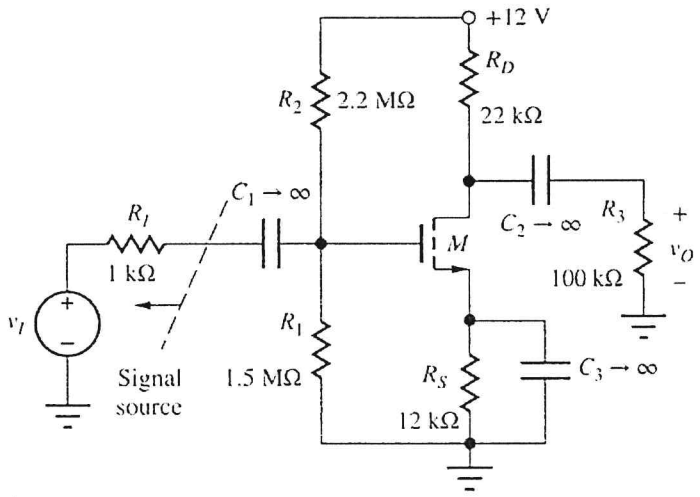

Figure 2. Common-source amplifier.

(a) Draw the AC small signal equivalent circuit of the amplifier and simplify it.

(10 marks)

(b) Calculate the voltage gain of the amplifier.

(5 marks)

(c) Determine the input resistance of the amplifier.

(5 marks)

(d) Calculate the maximum input signal level.

(5 marks)

Question 4

An active low-pass filter is a circuit that uses an op-amp to allow low-frequency signals to pass while attenuating higher frequencies. Design an active low-pass filter (choose the values of R_1, R_2, and C) with f_H = 2 kHz, R_{in} = 5 kΩ, and A_v = -100.

(a) Determine the value of the resistors required.

(5 marks)

(b) Determine the value of the capacitor required.

(5 marks)

(c) Draw the architecture of the low-pass filter.

(5 marks)

(d) Sketch the frequency response of the designed filter.

(5 marks)

(e) Modify the filter to high pass filter and draw its architecture.

(5 marks)

Question 5

Figure 3 shows a Brokaw bandgap reference circuit that produces an output voltage of 5.000 V with zero temperature coefficient at a temperature of 47°C. The collector current is 25 μA, and I_S = 0.5 fA. The emitter area, A_{E1} is 2 μm^2 and A_{E2} is 20 μm^2.

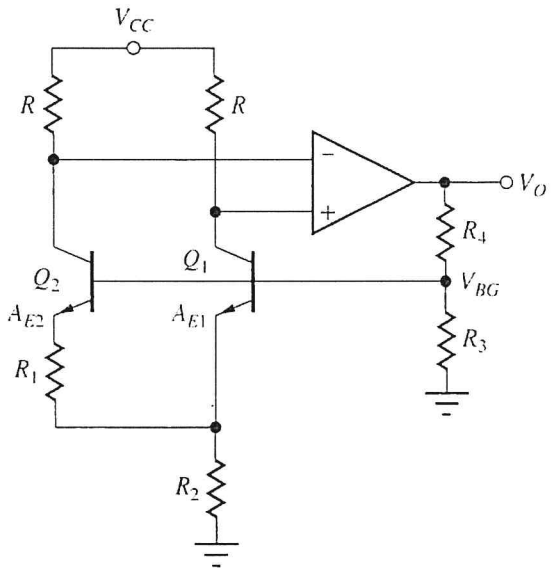

Figure 3: Bandgap reference circuit.

(a) Find the value of V_T.

(5 marks)

(b) Determine the value of V_{PTAT}.

(5 marks)

(c) Calculate the value of R_1 required for the design.

(5 marks)

(d) Find the value of R_2 needed.

(10 marks)

APPENDIX

Current-voltage equations of the nMOS Transistor:-

$I_D = 0$ for $V_{GS} < V_T$

$$I_D(lin) = \frac{k_n}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^{\ 2}\right] \quad \text{for } V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T$$

$$I_D(sat) = \frac{k_n}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad \text{for } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T$$

Where,

$$k_n = \mu_n C_{ox}\frac{W}{L}$$

Current-voltage equations of the pMOS Transistor:-

$I_D = 0$ for $V_{GS} > V_T$

$$I_D(lin) = \frac{k_p}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^{\ 2}\right] \quad \text{for } V_{GS} \leq V_T \text{ and } V_{DS} > V_{GS} - V_T$$

$$I_D(sat) = \frac{k_p}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad \text{for } V_{GS} \leq V_T \text{ and } V_{DS} \leq V_{GS} - V_T$$

Where,

$$k_p = \mu_p C_{ox}\frac{W}{L}$$

Threshold voltage:-

$$V_T(V_{SB}) = V_{T0} + \gamma(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|})$$

Capacitance Current:-

$$i_c = C_{load}\frac{dV_{out}}{dt}$$

END OF EXAMINATION PAPER