UNIVERSITI KUALA LUMPUR
KAMPUS CAWANGAN MALAYSIAN SPANISH INSTITUTE

FINAL EXAMINATION

OCTOBER 2025 SEMESTER

COURSE CODE	: SAB24803
COURSE NAME	: ANALOG CIRCUIT APPLICATIONS 2
PROGRAMME LEVEL	: BACHELOR
DATE	: 30 JANUARY 2026
TIME	: 9.00AM – 12.00PM
DURATION	: 3 HOURS

INSTRUCTIONS TO CANDIDATES

1. Please CAREFULLY read the instructions given in the question paper.
2. This question paper has information printed on both sides of the paper.
3. This question paper consists of FIVE (5) questions. Answer FOUR (4) questions ONLY.
4. Answer all questions in English language ONLY.

THERE ARE 5 PAGES OF QUESTIONS, EXCLUDING THIS PAGE.

Question 1

Figure 1 shows the energy band diagrams of Semiconductors A, B, and C. E_C, E_V, and E_{Fi} are the conduction bands, valence bands, and intrinsic Fermi level, respectively. E_D is the donor level and E_A is the acceptor level. Based on the figure, answer the following questions:

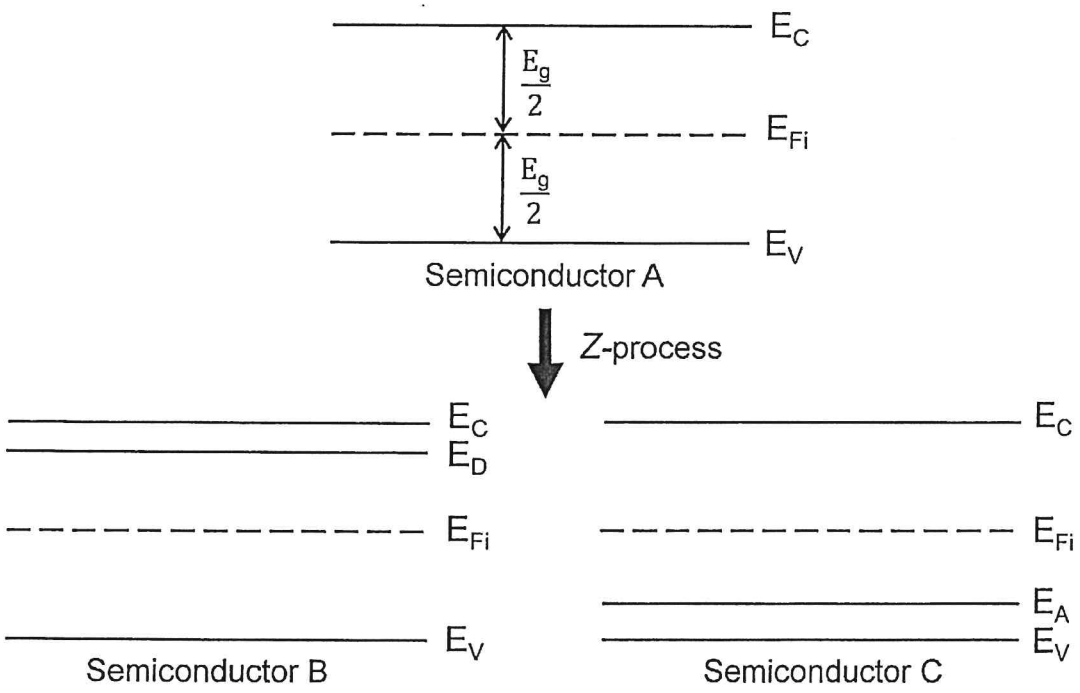

Figure 1 Energy band diagram.

a) State the type of Semiconductor A, B, and C.

(5 marks)

b) Determine the majority and minority carriers of Semiconductors B and C, respectively.

(8 marks)

c) Define the Z-process as shown in Figure 1. Then, briefly explain the formation of Semiconductors B and C. Assume that Semiconductor A is Silicon.

(12 marks)

Question 2

a) For ideal diodes, show the voltage waveforms across the secondary winding and across R_L when a 230 V_{rms} sine wave is applied to the primary winding in Figure 2.

(10 marks)

b) What is minimum peak inversion voltage (PIV) rating must the diode have?

(5 marks)

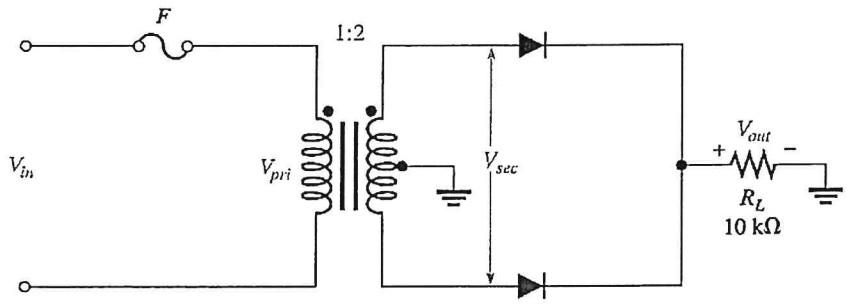

Figure 2 A centre-tapped full-wave rectifier.

c) Figure 3 shows a basic Zener diode regulator circuit. What is the smallest load resistor that can be used before losing regulation? Assume an ideal Zener diode model and V_{IN} = 20 V.

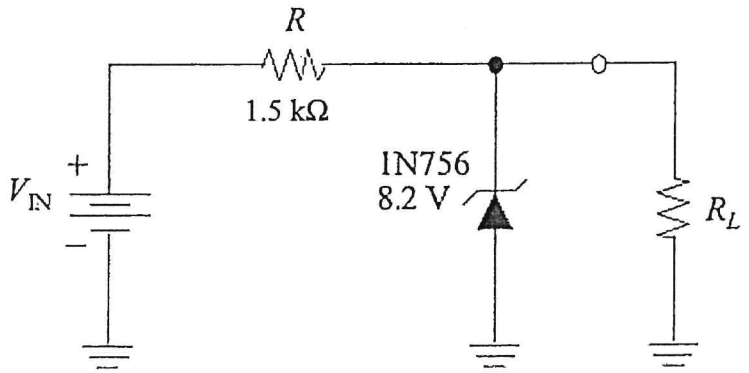

Figure 3 A basic Zener diode regulator circuit.

(10 marks)

Question 3

Figure 4 shows an npn bipolar junction transistor (BJT) in a simple circuit. In this configuration, the transistor is biased in active mode and has a current gain of $\beta_{DC} = 50$. The BJT is of Silicon with $V_{BE} = 0.7$ V. Given $I_B = 0.1$ mA.

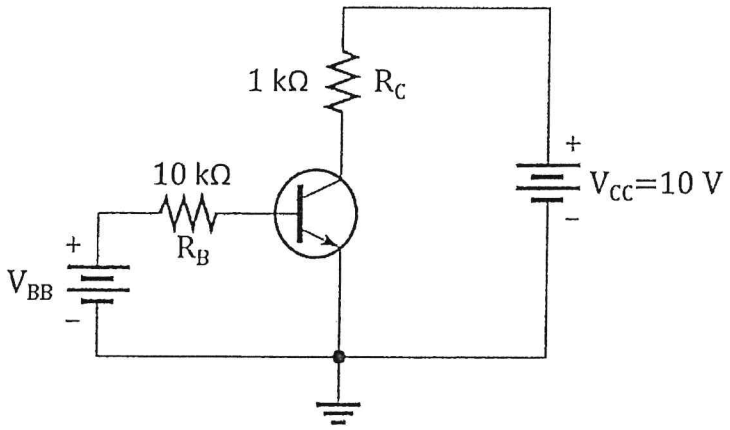

Figure 4 An npn BJT in a common-emitter circuit configuration.

a) For the transistor circuit in Figure 4, what is V_{CE} when $V_{BB} = 0$ V.

(4 marks)

b) What is the saturation current of the BJT circuit? Neglect $V_{CE(sat)}$.

(4 marks)

c) Is the transistor saturated? Justify.

(2 marks)

d) Plot the DC load line of the transistor circuit and determine its operating point (Q-point).

(15 marks)

Question 4

Figure 5 shows a common emitter amplifier with a voltage divider biasing. The common emitter amplifier has a variable gain control, using a 150 Ω potentiometer for R_E with the wiper ac grounded. As the potentiometer is adjusted, more or less of R_E is bypassed to the ground at the signal frequency, thus varying the gain. The total R_E remains constant to dc because the capacitor is an open to dc, keeping the bias fixed. Given V_T = 26 mV at room temperature and V_A = 100 V.

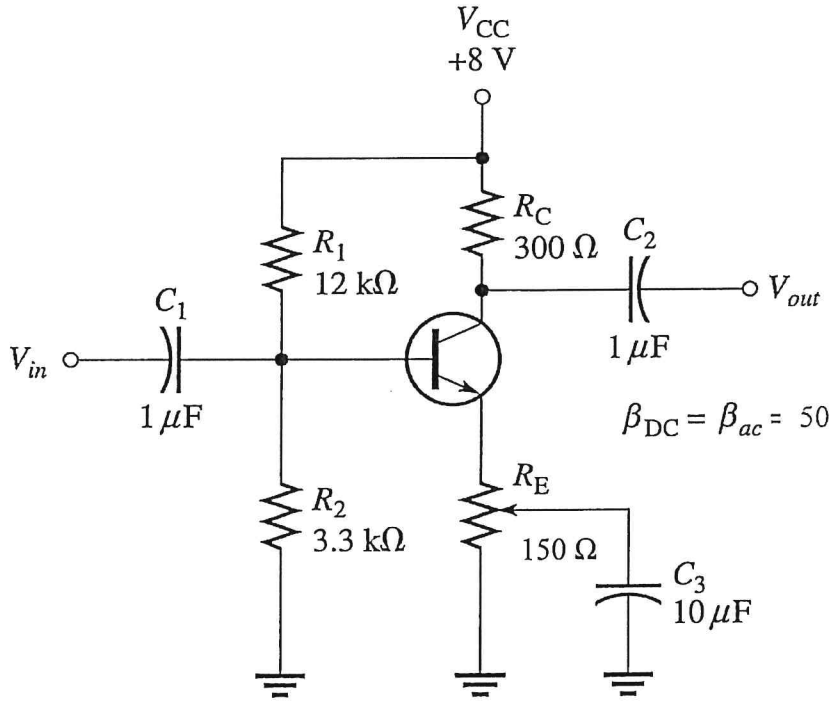

Figure 5 A common emitter amplifier with a voltage divider biasing circuit.

a) Determine the maximum and the minimum gain for the amplifier.

(20 marks)

b) If a load resistance of 600 Ω is placed on the output of the amplifier in Figure 5, what is the maximum gain?

(5 marks)

Question 5

An n-channel enhancement mode Metal Oxide Semiconductor Field Effect Transistor (MOSFET) operating with V_{GS} = 1.5 V and V_{DS} = 2.0 V has the following parameters:

Oxide thickness: 15 nm
Electron mobility: 450 cm^2/V-s
Threshold voltage: 0.7 V
Width-to-length (W/L) ratio: 30

a) Determine whether the MOSFET is operating in the saturation or non-saturation region.

(2 marks)

b) Calculate the drain current, I_D.

(10 marks)

c) If the channel length modulation parameter λ = 0.03 V^{-1}, determine the corrected drain current I_D taking into account the channel length modulation.

(10 marks)

d) Compare the answers obtained in (b) and (c), and explain the difference.

(3 marks)

END OF EXAMINATION PAPER