UNIVERSITI KUALA LUMPUR
KAMPUS CAWANGAN MALAYSIAN SPANISH INSTITUTE

FINAL EXAMINATION
OCTOBER 2025 SEMESTER

COURSE CODE	: SAB 23203
COURSE NAME	: INTRODUCTION TO VLSI AND FABRICATION
PROGRAMME LEVEL	: BACHELOR
DATE	: 24 JANUARY 2026
TIME	: 02.00 PM – 4.30 PM
DURATION	: 2 HOURS 30 MINUTES

INSTRUCTIONS TO CANDIDATES

1. Please read the instructions given in the question paper CAREFULLY.
2. This question paper consists of FIVE (5) QUESTIONS.
3. Answer FOUR (4) questions only.
4. Please write the answer in the answer booklet provided.
5. Answer all questions in English language ONLY.

THERE ARE 4 PAGES OF QUESTIONS, EXCLUDING THIS PAGE.

Question 1

The enhancement-mode MOSFET behaves as a "normally open" switch, requiring a gate-to-source voltage to turn on the device. Sketch and label the cross-sectional view of an n-channel (NMOS) transistor, clearly indicating the pinch-off region and the equations under the following operating conditions:

(a) Linear region.

(5 marks)

(b) Edge of saturation.

(10 marks)

(c) Beyond saturation.

(10 marks)

Question 2

A transistor-level CMOS logic circuit has a function of $F = \overline{x + wyz}$. By using the least number of transistors:

(a) Identify the nMOS portion of the circuit and then implementing this equation as a **2-input gate-level** schematic.

(5 marks)

(b) Apply bubble pushing on the **2-input gate-level** schematic in (a) to construct the gate-level schematic for the pMOS portion of the circuit.

(5 marks)

(c) Use the gate-level schematic in (a) and (b) to construct the **transistor-level** schematic for the function.

(15 marks)

Question 3

Figure 1 shows the symbol of a CMOS logic gate.

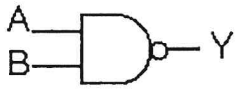

Figure 1: Symbol of a logic gate.

(a) Identify the logic gate and write its equation.

(5 marks)

(b) Draw the layout of the logic gate.

(5 marks)

(c) Draw the stick diagram of the logic gate.

(5 marks)

(d) Draw the timing diagram of the logic gate.

(5 marks)

(e) Draw the transistor level diagram.

(5 marks)

Question 4

Consider a layout shown in Figure 2. The parameters of the NMOS transistor is as shown in the layout. Given, $V_{DD} = 3.3V, V_{T0,n} = 0.4V, \mu_n C_{ox} = 100\mu A/V^2$. Neglect the channel-length modulation and substrate bias effect $(\lambda = 0, \gamma = 0)$ and the $V_{GS} = 1.0V$. Assume it operates in saturation.

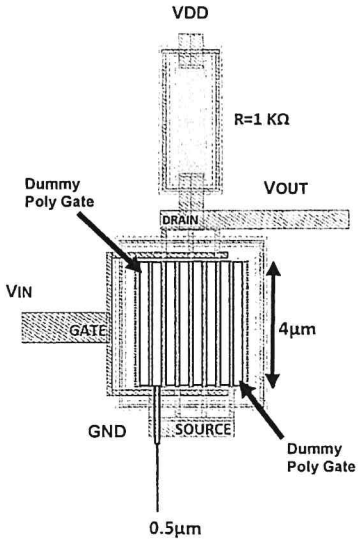

Figure 2: Layout for Question 4.

(a) Construct the schematic from the layout.

(5 marks)

(b) Determine the value of I_d.

(10 marks)

(c) Determine the value of V_{DS}.

(5 marks)

(d) Prove the assumption that it operates in saturation.

(5 marks)

Question 5

The simplified layout of a transistor in a 0.5µm process is shown in Figure 3 with the fabricated dimensions. Determine the device parasitics below using the following process model values of Cox = 1.8fF/µm², Cj = 0.75fF/µm² and Cjsw = 0.25 fF/µm.

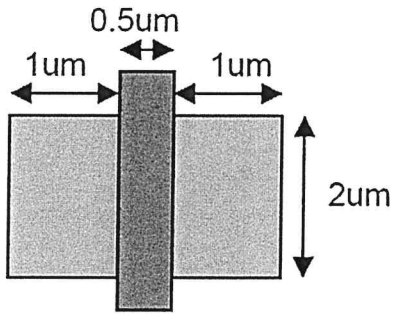

Figure 3. Simplified layout of a transistor.

(a) Determine the gate capacitance, C_G.

(5 marks)

(b) Find the gate-to-drain capacitance, C_{GD}.

(5 marks)

(c) Determine the drain-to-bulk capacitance, C_{DB}.

(5 marks)

(d) Determine the total capacitance at the drain node.

(5 marks)

(e) If the drain node RC time constant is 4psec, find its channel resistance.

(5 marks)

APPENDIX

Current-voltage equations of the nMOS Transistor:-

$I_D = 0$ for $V_{GS} < V_T$

$$I_D(lin) = \frac{k_n}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^{\ 2}\right] \quad \text{for } V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T$$

$$I_D(sat) = \frac{k_n}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad \text{for } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T$$

Where,

$$k_n = \mu_n C_{ox}\frac{W}{L}$$

Current-voltage equations of the pMOS Transistor:-

$I_D = 0$ for $V_{GS} > V_T$

$$I_D(lin) = \frac{k_p}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^{\ 2}\right] \quad \text{for } V_{GS} \leq V_T \text{ and } V_{DS} > V_{GS} - V_T$$

$$I_D(sat) = \frac{k_p}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad \text{for } V_{GS} \leq V_T \text{ and } V_{DS} \leq V_{GS} - V_T$$

Where,

$$k_p = \mu_p C_{ox}\frac{W}{L}$$

Threshold voltage:-

$$V_T(V_{SB}) = V_{T0} + \gamma(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|})$$

Capacitance Current:-

$$i_c = C_{load}\frac{dV_{out}}{dt}$$

END OF EXAMINATION PAPER