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CONFIDENTIAL

SET A

UNIVERSITI KUALA LUMPUR

MALAYSIA FRANCE INSTITUTE

FINAL EXAMINATION

JULY 2010 SESSION

SUBJECT CODE	: FLD 20402
SUBJECT TITLE	: DIGITAL SYSTEM
LEVEL	: DIPLOMA
DURATION	: 12.30pm – 2.30pm (2 HOURS)
DATE / TIME	: 10 NOVEMBER 2010

INSTRUCTIONS TO CANDIDATES

1. Please read the instructions given in the question paper CAREFULLY.
2. This question paper is printed on both sides of the paper.
3. Please write your answers on the answer booklet provided.
4. Answers should be written in blue or black ink except for sketching, graphic and illustration.
5. This question paper consists of TWO (2) sections. Section A and B. Answer all questions in Section A. For Section B, answer two (2) questions only.
6. Answer all questions in English.

THERE ARE 5 PRINTED PAGES OF QUESTIONS, EXCLUDING THIS PAGE.

SECTION A (Total: 60 marks)

INSTRUCTION: Answer ALL questions.
Please use the answer booklet provided.

Question 1

(a) Define four types of flip-flops.

(4 marks)

(b) Define overflow and state the two rules for determining whether overflow has occurred.

(3 marks)

(c) Form an Exclusive OR from NANDs.

(2 marks)

(d) Describe an encoder.

(2 marks)

(e) Convert the following negative decimal number to two's complement 8 bit number:

i. -10

(1 marks)

ii. -30

(1 marks)

iii. -100

(1 marks)

(f) Solve the problems below in binary numbers.

i. Compute 01101010 x 01110111. Show your work.

(2 marks)

ii. 011011000 divided by 01011. Show your work.

(2 marks)

iii. Compute 42 – 137 in binary. Show your work.

(2 marks)

Question 2

Figure 1, shows an asynchronous counter circuit.

(a) Define a positive edge triggered clock and a negative edge triggered clock.

(2 marks)

(b) Determine the modulus of this counter.

(2 marks)

(c) Determine the sequence of states in a truth table.

(5 marks)

(d) Draw the complete timing diagram for 8 clock pulses.

(5 marks)

(e) Modify this circuit, so that this up-counter can count from 0-1-2-3-4-5-6-7-8-9-0-1-2-3-4-5-6-7-8-9..and so on.

(6 marks)

A four-bit "up" counter

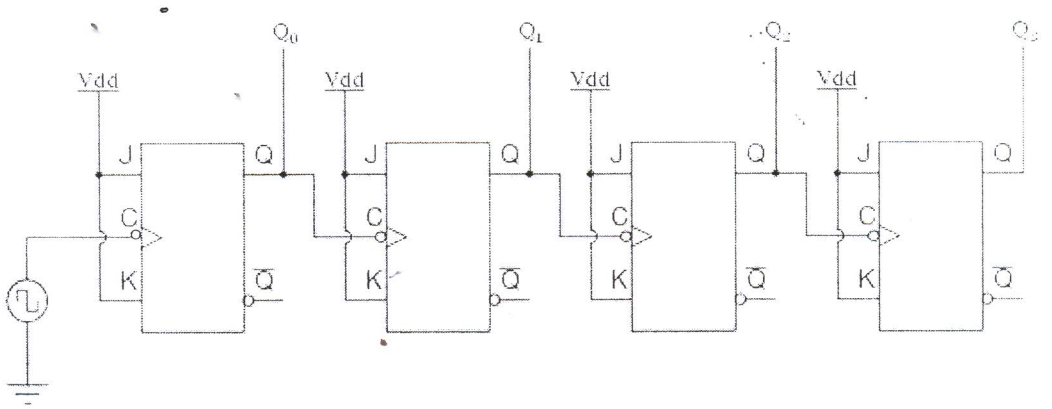

Figure 1

Question 3

Refer to **Figure 2**.

(a) Show the truth table for clocked SR type flip flop.

(3 marks)

(b) Construct a clocked SR type flip flop from NAND gate and NOR gate.

(5 marks)

(c) State the main function of this flip flop.

(2 marks)

(d) Determine the output waveform of Q.

(5 marks)

(e) Determine the output waveform of $\overline{Q}$.

(5 marks)

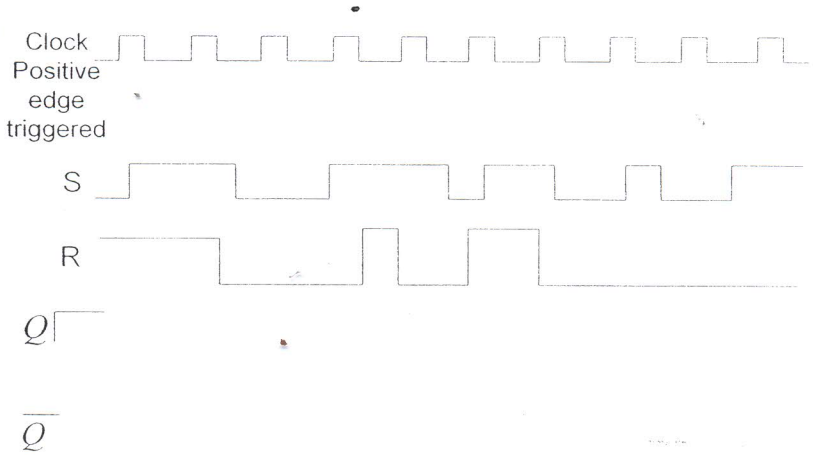

Figure 2

SECTION B (Total: 40 marks)

INSTRUCTION: Answer TWO (2) questions only
Please use the answer booklet provided.

Question 4

Binary Coded Decimal (BCD) is a way to store decimal numbers in binary form. The number representation requires 4 bits to store every decimal digit from 0 to 9. Since there are 10 different combinations of BCD, we need at least a 4 bit of Gray Code to create sufficient number of these combinations.

Design a Gray Code to BCD code converter based on the following procedures:

(a) Compute the truth table of the converter.

(8 marks)

(b) Apply Karnaugh Map to look for the minimized logic expression.

(8 marks)

(c) Implement the logic gates or draw the schematic diagram

(4 marks)

Question 5

Visualize a full adder function of a 3-bit binary input and;

(a) Construct the truth table

(6 marks)

(b) Indicate the sum-of-product expressions

(4 marks)

(c) Determine the Karnaugh Map

(6 marks)

(d) Draw the circuit.

(4 marks)

Question 6

Refer to **Figure 3**.

(a) Determine the expression of F.

(5 marks)

(b) Summarize the expression of F.

(10 marks)

(c) Convert the summarized expression of F into Nand gate implementation only.

(5 marks)

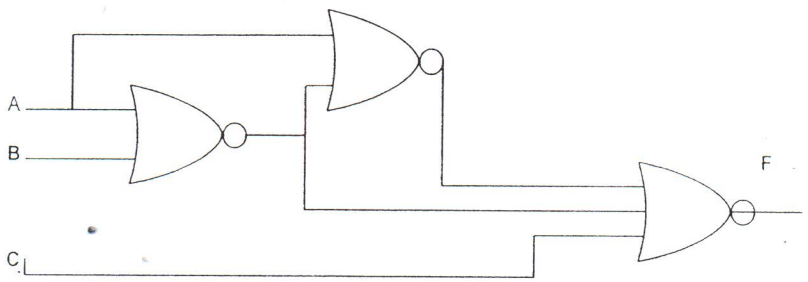

Figure 3

END OF QUESTION PAPER