CONFIDENTIAL

# UNIVERSITI KUALA LUMPUR
## Malaysian Institute of Marine Engineering Technology

## FINAL EXAMINATION

## FEBRUARY 2025 SEMESTER SESSION

| | | |
|---|---|---|
| **SUBJECT CODE** | : | **LED22002** |
| **SUBJECT TITLE** | : | **DIGITAL ELECTRONICS** |
| **PROGRAMME NAME** (FOR MPU: PROGRAMME LEVEL) | : | **DIPLOMA OF ENGINEERING TECHNOLOGY IN ELECTRICAL AND ELECTRONICS (MARINE)** |
| **TIME / DURATION** | : | **09.00 AM - 12.00 PM (3 HOURS)** |
| **DATE** | : | **23 JUNE 2025** |

### INSTRUCTIONS TO CANDIDATES

1. Please read **CAREFULLY** the instructions given in the question paper.
2. This question paper has information printed on both sides of the paper.
3. Answer only **FOUR (4)** questions.
4. Please write your answers on this answer booklet provided.
5. Answer **ALL** questions in English language **ONLY**.
6. Write your answer in black or blue ink.

**THERE ARE 4 PAGES OF QUESTIONS, EXCLUDING THIS PAGE.**

**INSTRUCTION: Answer FOUR (4) questions only.**
**Please use the answer booklet provided.**

**Question 1**
**(Refer to Boolean Algebra and Logic Simplification)**

Assuming that a liquid tank sensor functions to monitor the liquid level, either in a HIGH or LOW condition. The sensor has three input compartments: A, B, and C. The tank has one output, known as "O". The output of the sensor will be HIGH only if the input follows these OPERATION CONDITIONS:

***OPERATION CONDITION: MORE THAN one of input is HIGH***

i. Construct the Truth Table based on the liquid tank OPERATION CONDITION,
(4 marks)

ii. Express the Boolean Expression following results in (i) and write the simplified equation,
(4 marks)

iii. Design the logic circuit for the simplified equation,
(6 marks)

iv. Produce the equivalent logic decoder circuit for the simplified circuit,
(5 marks)

v. Design the suitable MUX to show the output, O during the operation condition.
(6 marks)

**Question 2**
**(Refer to Latches, Flip-Flops)**

Design a synchronous counter with the binary down count sequence shown in the state diagram in Figure 1. Use J-K Flip-Flop, Negative Going Transition (NGT) clock. Thus, determine the following:

i. The transition state table
(5 marks)

ii. Boolean Equations for JK inputs
(5 marks)

iii. Simulation of the circuit for the counter using a software to show the output waveform.

(15 marks)

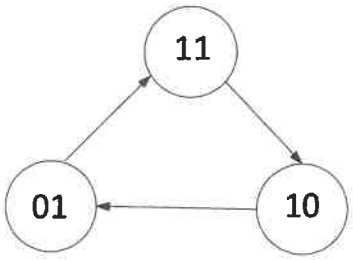


Figure 1: State Diagram

**Question 3**
**(Refer to the Functions of Combinational Logic).**

a) In digital electronics, minimum terms and maximum terms are associated with the outputs based on possible combinations of inputs, P, Q and R as shown in Table 1. Produce all the minimum terms and maximum term notations for X0.

(6 marks)

Table 1

| P | Q | R | X0 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

(b) On board ship, an engineer needs to operate a digital equipment which consists of a coded data. Translate the following information into their decimal equivalent that need to be displayed on the screen.

i. $0010\ 1010_2$ to decimal

(3 marks)

ii. $29_{10}$ to the binary number system

(3 marks)

iii. $1001\ 0110\ 0000\ 1110_2$ to hexadecimal

(3 marks)

(c) Determine the Boolean equation for the output, F shown in Figure 1. Assuming A, B and C are the inputs of the circuit.

(5 marks)

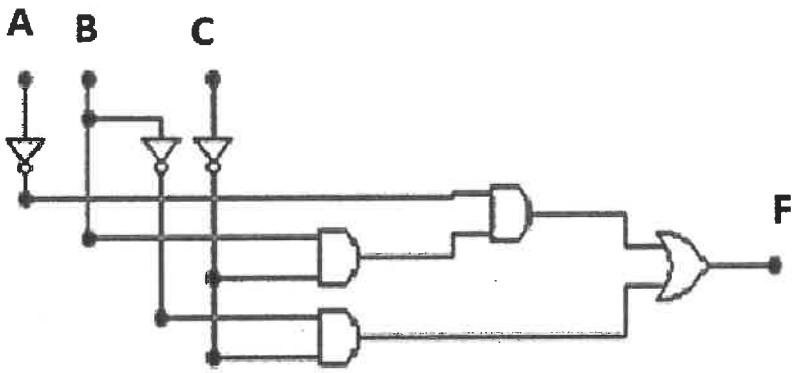


Figure 1: Combinational Logic Gates

(d) Figure 2 shows the waveform pattern that represents output X. Produce the respective truth table if A and B are the inputs for the device.

(5 marks)

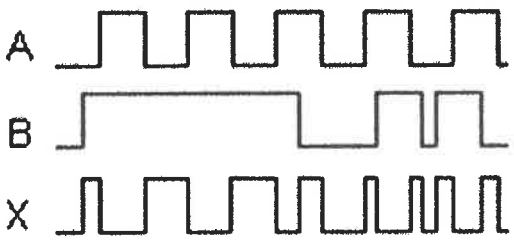


Figure 2: Inputs and Output waveforms

**Question 4**
**(Refer to Asynchronous / synchronous counter )**

(a) It is possible to implement any logic expression using only NAND gates or NOR gates and no other type of gate. Produce the equivalent circuit and redraw, shown in Figure 3 by using NAND gates ONLY.

(10 marks)

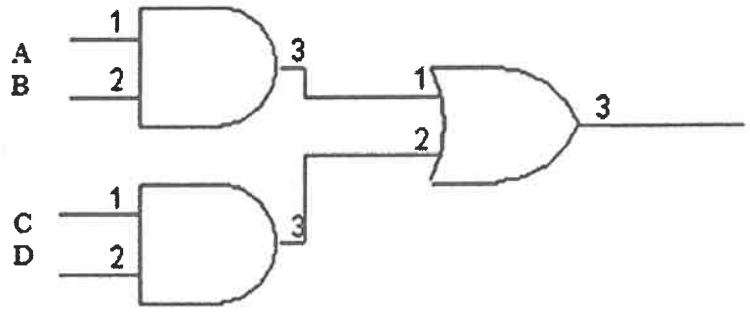


Figure 3: Basic Equivalent Circuit

(b) The origins of many sailor's superstitions are based on the routes of **F** and **N.** Thus, calculate all common routes at their simplest form.

i. $F = \overline{A}\overline{B}C + \left(\overline{A + B + \overline{C}}\right) + A\overline{B}\overline{C}$

(5 marks)

ii. N = $\overline{\overline{A + BC}} + \overline{AB}(AB + BB)$

(5 marks)

(c) Multiplexer is the device which has n inputs and only one output. Figure 4 shows 4x1 multiplexer that has four data inputs $I_3$, $I_2$, $I_1$ and $I_0$, two selection lines $s_1$ and $s_0$ and one output, Y. Determine the truth table of the 4-to-1 multiplexer.

(5 marks)

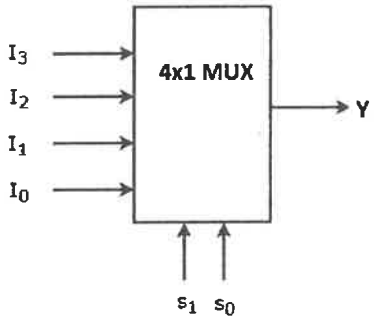


Figure 4

**Question 5**

**(Refer to the Functions of Combination Logic).**

a) With the aid of diagram, state the main difference between combination logic circuit and sequential logic circuit.

(4 marks)

b) Design MOD-6 asynchronous count up counter using preset and clear J-K flip flop. The design should include the following:

i. The state diagram.

(6 marks)

ii. The complete counter circuit.

(15 marks)

**END OF EXAMINATION QUESTION**