CONFIDENTIAL

UNIVERSITI KUALA LUMPUR
Malaysian Institute of Marine Engineering Technology

FINAL EXAMINATION
FEBRUARY 2025 SEMESTER SESSION

SUBJECT CODE	:	**LED12203**
SUBJECT TITLE	:	**ANALOGUE AND DIGITAL ELECTRONICS**
PROGRAMME NAME (FOR MPU: PROGRAMME LEVEL)	:	**DIPLOMA OF ENGINEERING TECHNOLOGY IN ELECTRICAL AND ELECTRONICS (MARINE)**
TIME / DURATION	:	**09.00AM – 12.00PM (3 HOURS)**
DATE	:	**25 JUNE 2025**

INSTRUCTIONS TO CANDIDATES

1. **Please CAREFULLY read the instructions given in the question paper.**
2. **This question paper has information printed on both sides of the paper.**
3. **This question paper consists of TWO (2) Sections; Section A and Section B.**
4. **Answer ALL questions in Section A. For Section B, answer TWO (2) questions.**
5. **Please write your answers on the answer booklet provided.**
6. **Answer all questions in English language only.**
7. **Formula has been appended for your reference.**

THERE ARE 6 PAGES OF QUESTIONS, EXCLUDING THIS PAGE.

SECTION A (Total: 60 marks)

INSTRUCTION: Answer ALL questions.
Please use the answer booklet provided.

Question 1

With reference to Operational Amplifiers (op-amp):

(a) Define slew rate of an op-amp.

(2 marks)

(b) Briefly explain **THREE (3)** disadvantages an op-amp circuit without negative feedback.

(6 marks)

(c) Describe the op-amp output impedance.

(4 marks)

(d) Describe the common mode connection of an op-amp.

(4 marks)

(e) Describe the method to compensate bias current in a voltage-follower circuit.

(4 marks)

Question 2

With reference to Counters:

(a) List **TWO (2)** basic types of state machines.

(4 marks)

(b) Explain the term asynchronous meaning in relation to counters.

(4 marks)

(c) Identify the number of flip-flops required to design a modulus-14 counter.

(2 marks)

(d) Explain the the function of the preset feature of counters such as the 74HC163 4-bit synchronous binary counter.

(2 marks)

(e) Describe the purpose of the ENP and ENT inputs and the RCO output for the 74HC163 4-bit synchronous binary counter.

(6 marks)

(f) Define up/down counter.

(2 marks)

Question 3

With reference to Latches, Flip-Flops, and Timers:

(a) Describe a latch.

(5 marks)

(b) List **TWO (2)** types of edge-triggered flip-flops.

(4 marks)

(c) Describe the propagation delay time.

(6 marks)

(d) Describe the briefly on a one-shot.

(5 marks)

SECTION B (Total: 40 marks)

INSTRUCTION: Answer TWO (2) questions ONLY.
Please use the answer booklet provided.

Question 4

With reference to BJT Amplifiers:

(a) Figure 1 shown the common-emitter amplifier that has ac emitter resistance, $r_e' = 10\ \Omega$ and total input resistance, $R_{in(tot)} = 5\ k\Omega$.

Determine:

i. the attenuation. (2 marks)

ii. the voltage gain, A_v. (4 marks)

iii. the overall voltage gain, A'_v. Give your answer in decibel. (4 marks)

iv. the peak voltage at the collector. (4 marks)

(b) A differential amplifier stage has collector resistors of $7.5\ k\Omega$ each. Determine the differential output voltage if $I_{C1} = 2\ mA$ and $I_{C2} = 1.5\ mA$. (6 marks)

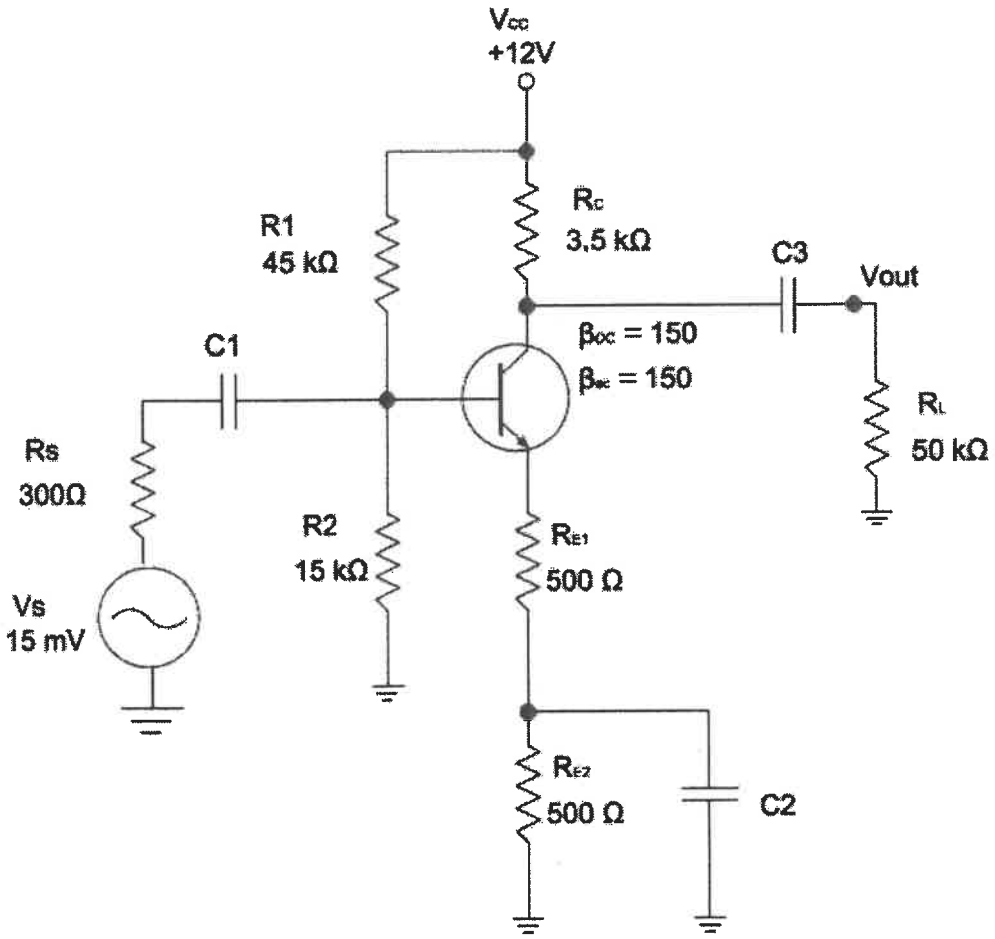


Figure 1

Question 5

With reference to Functions of Combinational Logic.

(a) Analyse the circuit's logical operation to determine the complete sum for parallel adder shown in Figure 2. Verify your result by longhand addition of the two input numbers.

(6 marks)

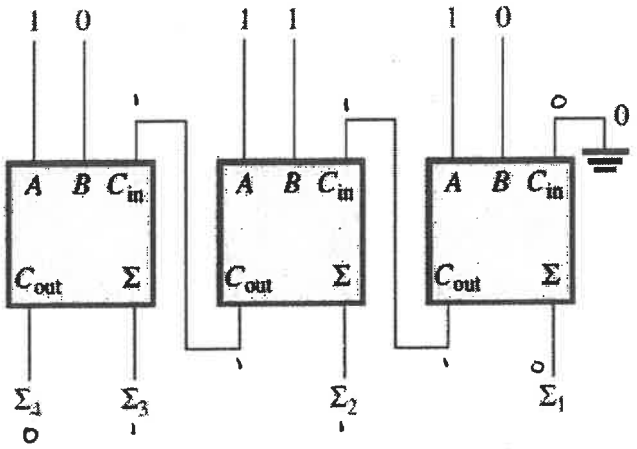


Figure 2

(b) The waveforms in Figure 3 are applied to the comparator as shown. Determine the output (A = B) waveform.

(6 marks)

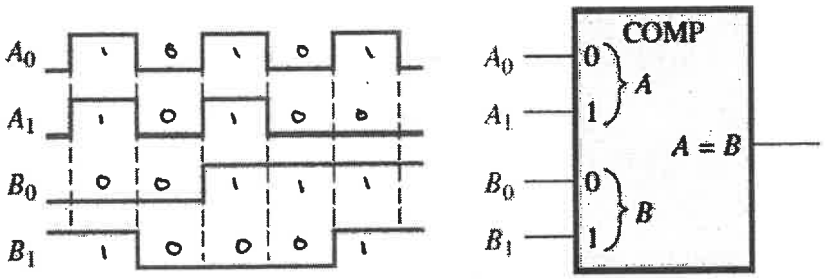


Figure 3

(c) Show the decoding logic circuit for the binary code A=1110110 if an active-HIGH (1) output.

(8 marks)

Question 6

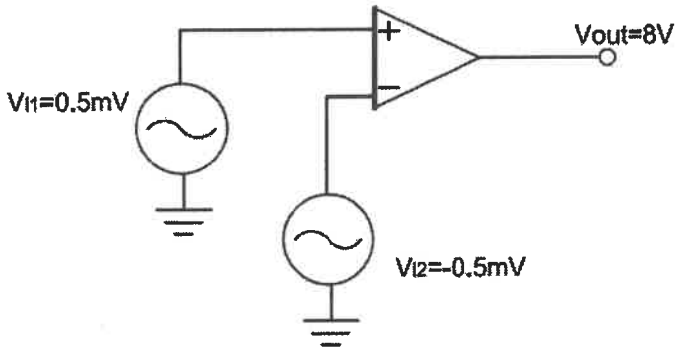
With reference to Power Amplifier and Shift Register.

(a) Each of four cascaded amplifier stages has 20 dB voltage gain respectively. Determine the overall voltage gain in dB and the actual overall voltage gain.

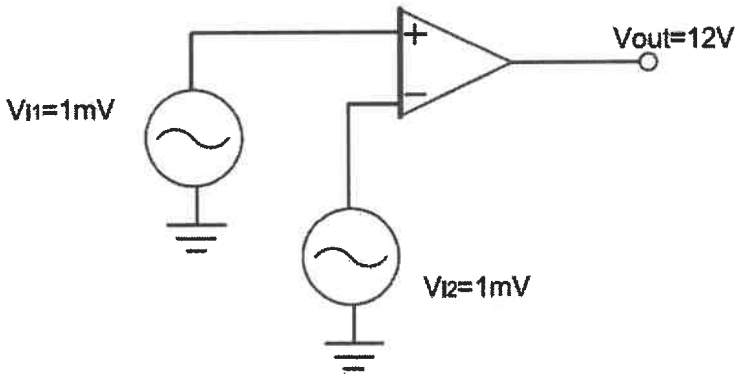
(5 marks)

(b) Calculate the CMRR of the circuit measurement shown in Figure 4. Give the answer in decibel.

(5 marks)



(a)



(b)

Figure 4

(c) Draw the logic diagram for modulus-4 Johnson counter using D flip-flop and write the sequence tabular.

(10 marks)

END OF EXAMINATION PAPER

List of Formulae

– LED12203 ANALOGUE AND DIGITAL ELECTRONICS (V2)

NO.	FORMULA
Common-Emitter	
1.	$r_e' \cong \frac{25mV}{I_E}$
2.	$R_{in(base)=\beta_{ac} r_e'}$
3.	$R_{in(tot)} = R_1 \| \| R_2 \| \| R_{in(base)}$
4.	$R_{out} \cong R_c$
5.	$A_v = \frac{R_c}{r_e'}$
6.	$A_i = \frac{I_c}{I_s}$
7.	$A_p = A_v' A_i$
8.	$Attenuation = \frac{V_s}{V_b} = \frac{R_s + R_{in(tot)}}{R_{in(tot)}}$
9.	$A_v' = \left(\frac{1}{Attenuation}\right) A_v$
Common-Collector	
10.	$A_v = \frac{R_e}{r_e' + R_e} \approx 1$
11.	$R_{in(base)} = \beta_{ac}(r_e' + R_e) \cong \beta_{ac} R_e$
12.	$R_{out} \cong \left(\frac{R_s}{\beta_{ac}}\right) \| \| R_E$
13.	$A_i = \frac{I_e}{I_{in}}$
14.	$A_p = \frac{R_{in(tot)}}{R_L} \cong A_i$
15.	$R_{in(base)} = \beta_{ac1}\beta_{ac2}(r'e + R_e)$
Common-Base	
16.	$A_v \cong \frac{R_c}{r_e'}$
17.	$R_{in(emitter)} \cong r_e'$
18.	$R_{out} \cong R_c$
19.	$A_i \cong 1$
20.	$A_p \cong A_v$
Multistage Amplifier	
21.	$A_v' = A_{v1} A_{v2} A_{v3} \dots A_{vn}$
22.	$A_{v(dB)} = 20 log A_v$
Differential Amplifier	
23.	$CMRR = \frac{A_{v(d)}}{A_{cm}}$
24.	$CMRR = 20log\left(\frac{A_{v(d)}}{A_{cm}}\right)$
Class A Power Amplifier	
25.	$A_p = \frac{P_L}{P_{in}}$
26.	$A_p = A_v^2\left(\frac{R_{in}}{R_L}\right)$
27.	$P_{DQ} = I_{CQ} V_{CEQ}$
28.	$P_{out)\max)} = 0.5 I_{CQ} V_{CEQ}$
Class B/AB Push-Pull Amplifiers	
29.	$I_{c(sat)} = \frac{V_{CC}}{R_L}$

List of Formulae

– LED12203 ANALOGUE AND DIGITAL ELECTRONICS (V2)

30.	$P_{out} = 0.25 I_{c(sat)} V_{CC}$
	Class C Amplifier
31.	$P_{out} = \frac{0.5 V_{CC}^2}{R_c}$
32.	$\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}}$
33.	$P_{D(avg)} = \left(\frac{t_{on}}{T}\right) P_{D(on)} = \left(\frac{t_{on}}{T}\right) I_{c(sat)} V_{ce(sat)}$
	Comparator
34.	$V_{UTP} = \frac{R_2}{R_1 + R_2}(+V_{out(max)})$
35.	$V_{LTP} = \frac{R_2}{R_1 + R_2}(-V_{out(max)})$
36.	$V_{HYS} = V_{UTP} - V_{LTP}$
	Summing Amplifier
37.	$V_{OUT} = -(V_{IN1} + V_{IN2} + \cdots + V_{INn})$
38.	$V_{OUT} = -\frac{R_f}{R_{IN}}(V_{IN1} + V_{IN2} + \cdots + V_{INn})$
39.	$V_{OUT} = -\left(\frac{R_f}{R_{IN1}} V_{IN1} + \frac{R_f}{R_{IN2}} V_{IN2} + \cdots + \frac{R_f}{R_{INn}} V_{INn}\right)$
	Integrator and Differentiator
40.	$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C}$

41.	$V_{out} = -\left(\frac{V_C}{t}\right) R_f C$
	Op-Amp Input Modes and Parameters
42.	$CMRR = \frac{A_{ol}}{A_{cm}}$
43.	$CMRR = 20log\left(\frac{A_{ol}}{A_{cm}}\right)$
44.	$I_{BIAS} = \frac{I_1 + I_2}{2}$
45.	$I_{OS} = \lvert I_1 - I_2 \rvert$
46.	$V_{OS} = I_{OS} R_{in}$
47.	$V_{OUT(error)} = A_v I_{OS} R_{in}$
48.	$Slew\ rate = \frac{\Delta V_{out}}{\Delta t}$
	Op-Amp Configurations
49.	$A_{cl(NI)} = 1 + \frac{R_f}{R_i}$
50.	$A_{cl(VF)} = 1$
51.	$A_{cl(I)} = -\frac{R_f}{R_i}$
	Op-Amp Impedances
52.	$Z_{in(NI)} = (1 + A_{ol} B) Z_{in}$
53.	$Z_{out(NI)} = \frac{Z_{out}}{1 + A_{ol} B}$
54.	$Z_{in(VF)} = (1 + A_{ol}) Z_{in}$
55.	$Z_{out(VF)} = \frac{Z_{out}}{1 + A_{ol}}$
56.	$Z_{in(I)} \cong R_i$

List of Formulae

– LED12203 ANALOGUE AND DIGITAL ELECTRONICS (V2)

57.	$Z_{out(I)} = \dfrac{Z_{out}}{1 + A_{ol}B}$
58.	$B = \dfrac{R_i}{R_i + R_f}$
Op-Amp Frequency Responses	
59.	$BW = f_{cu}$
60.	$\dfrac{V_{out}}{V_{in}} = \dfrac{1}{\sqrt{1 + f^2/f_c^2}}$
61.	$A_{ol} = \dfrac{A_{ol(mid)}}{\sqrt{1 + f^2/f_c^2}}$
62.	$\theta = -tan^{-1}\left(\dfrac{f}{f_c}\right)$
63.	$f_{c(cl)} = f_{c(ol)}\left(1 + BA_{ol(mid)}\right)$
64.	$BW_{cl} = BW_{ol}\left(1 + BA_{ol(mid)}\right)$
65.	$f_T = A_{cl}f_{c(cl)}$
Comparator	
66.	$V_{UTP} = \dfrac{R_2}{R_1 + R_2}\left(+V_{out(max)}\right)$
67.	$V_{LTP} = \dfrac{R_2}{R_1 + R_2}\left(-V_{out(max)}\right)$
68.	$V_{HYS} = V_{UTP} - V_{LTP}$
Summing Amplifier	
69.	$V_{out} = -(V_{IN1} + V_{IN2} + \cdots + V_{INn})$
70.	$V_{out} = -\dfrac{R_f}{R_{in}}(V_{IN1} + V_{IN2} + \cdots + V_{INn})$
71.	$V_{out} = -\left(\dfrac{R_f}{R_1}V_{IN1} + \dfrac{R_f}{R_2}V_{IN2} + \cdots + \dfrac{R_f}{R_n}V_{INn}\right)$
Integrator and Differentiator	
72.	$\dfrac{\Delta V_{out}}{\Delta t} = -\dfrac{V_{in}}{R_i C}$
73.	$V_{out} = -\left(\dfrac{V_c}{t}\right)R_f C$
Functions of Combinational Logic	
74.	Half-Adder: $C_{out} = AB$, $\sum = A \oplus B$
75.	Full-Adder: $\sum = (A \oplus B) \oplus C_{in}$, $C_{out} = AB + (A \oplus B)C_{in}$
76.	$C_g = AB$
77.	$C_p = A + B$
78.	$C_{out} = C_g + C_p C_{in}$
79.	$t_W = 0.7RC_{EXT}$
80.	$t_W = 0.32RC_{EXT}\left(1 + \dfrac{0.7}{R}\right)$
81.	$t_W = 1.1R_1C_1$

List of Formulae

– LED12203 ANALOGUE AND DIGITAL ELECTRONICS (V2)

Transition table for a J-K flip-flop.

Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

Q_N: present state
Q_{N+1}: next state
X: "don't care"

Transition table for a D flip-flop.

Output Transitions			Flip-Flop Input
Q_N		Q_{N+1}	D
0	⟶	0	0
0	⟶	1	1
1	⟶	0	0
1	⟶	1	1