UNIVERSITI KUALA LUMPUR
MALAYSIAN INSTITUTE OF MARINE ENGINEERING TECHNOLOGY

FINAL EXAMINATION
SEPTEMBER 2016 SEMESTER

COURSE CODE	: LEB 10403
COURSE NAME	: DIGITAL ELECTRONIC
PROGRAMME NAME (FOR MPU: PROGRAMME LEVEL)	: BACHELOR OF MARINE ELECTRICAL ELECTRONIC
DATE	: 16TH JANUARY 2017
TIME	: 2.00PM
DURATION	: 3 HOURS

INSTRUCTIONS TO CANDIDATES

1. Please CAREFULLY read the instructions given in the question paper.
2. This question paper has information printed on both sides of the paper.
3. This question paper consists of TWO (2) sections; Section A and Section B.
4. Answer ALL questions in Section A. For Section B, answer THREE (3) questions WITH AT LEAST ONE (1) question from question 4 or question 5.
5. Please write your answers on the answer booklet provided.
6. Answer all questions in English language ONLY.

THERE ARE 7 PAGES OF QUESTIONS, INCLUDING THIS PAGE.

SECTION A (Total: 40 marks)

INSTRUCTION: Answer ALL questions.
Please use the answer booklet provided.

Question 1

a) Convert the binary number below to their decimal equivalent. *(Course Learning Outcome 1)*

i. 01101011_2
ii. 10010101_2
iii. 11011110_2

[6 marks]

b) Convert the decimal number below to their BCD equivalent. *(Course Learning Outcome 1)*

i. 187_{10}
ii. 962_{10}, and
iii. 529_{10}

[6 marks]

c) Rewrite **Table Q1 (c)** below in you answer booklet. Fill in the table by indicating the 8 – bit sign – and – magnitude, 1's complement and 2's complement representation for each of the decimal number. *(Course Learning Outcome 1)*

Table Q1 (c)

Decimal	Sign – and – magnitude	1's complement	2's complement
+ 30			
+ 13			
- 6			
- 15			

[8 marks]

Question 2

a. Simplify the following Boolean expressions using Boolean algebra.
(Course Learning Outcome 2)

i. $W = (\bar{A} + B)C + ABC$

[3 marks]

ii. $X = AB + (\bar{A} + \bar{B})C + AB$

[3 marks]

b. Given the function F (A,B,C) = $(A + B)(C + \bar{B})$
(Course Learning Outcome 2)

i. Convert the given function to a standard sum – of – product (SOP) form.

[4 marks]

ii. Construct the truth table for the standard SOP form.

[4 marks]

iii. Draw the Karnaugh Map and express the simplified equation, and

[3 marks]

iv. Sketch the logic circuit of the simplified equation in (iii).

[3 marks]

SECTION B (Total: 60 marks)

INSTRUCTION: Answer THREE (3) ONLY from FOUR (4) questions.
Please use the answer booklet provided.

Question 3

a) Sketch the corresponding logic circuit diagram for the following expressions using **ONLY** AND gate, OR gate and INVERTER. *(Course Learning Outcome 2 & 3)*

i. $X = \overline{AB(C + \bar{D})}$

[4 marks]

ii. $Y = \overline{M + N} + (\bar{P}Q)$

[4 marks]

b) Derive and simplify the expression from the corresponding logic circuit diagram in **Figure Q3 (b).** *(Course Learning Outcome 2 & 3)*

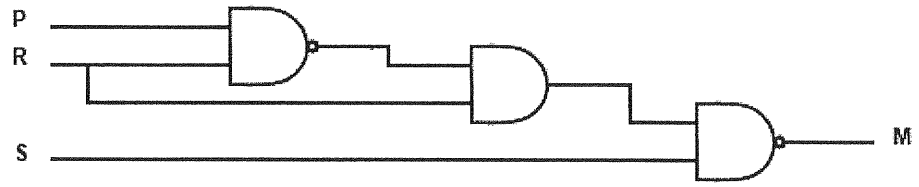

Figure Q3 (b)

[2 marks]

c) Derive and simplify the expression from the corresponding logic circuit diagram in **Figure Q3 (c).** *(Course Learning Outcome 2 & 3)*

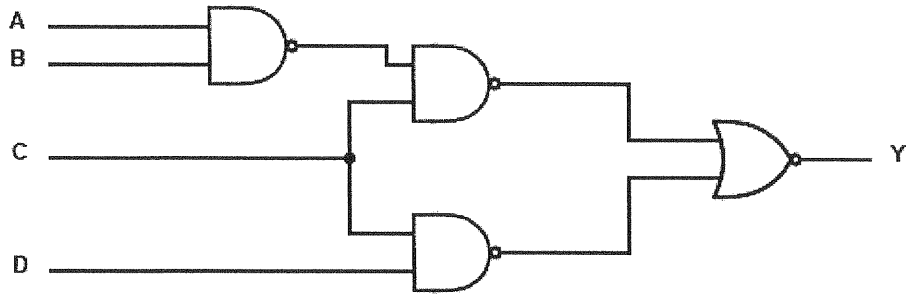

Figure Q3 (c)

[2 marks]

d) Draw the following expression **ONLY** by using **NAND gates**.
(Course Learning Outcome 2 & 3)

i. $X = ABC$
ii. $Y = \overline{EF} + \overline{GH}$

[8 marks]

Question 4

a) Produce all outputs shown in Table: 1 into a standard Sum-of-Product (SOP) format. *(Course Learning Outcome 3)*

X	Y	Z	Q
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Table: 1

[5 marks]

b) Given the function *F (A,B,C)* = $A\overline{C} + A\overline{BC} + A\overline{B} + \overline{A}B + \overline{A}BC + ABC$
(Course Learning Outcome 4)

i) Produce the truth table for the output, *F*

[3 marks]

ii) Use the Karnaugh Map and write the simplified Boolean expression

[3 marks]

iii) Draw the basic logic circuit for the simplified expression in part (b)(ii)

[3 marks]

iv) Express the output F, in sum-of-products (SOP) form, and

[3 marks]

v) Redraw the circuit in part (c) using NAND gates only.

[3 marks]

Question 5

a) Digital bits transmission can be done in serial or parallel. Describe the main differences between synchronous and asynchronous counters. *(Course Learning Outcome 5)*

[4 marks]

b) Design MOD 7 synchronous count up counter by using JK flip flop. Take the negative going transition clock (NGT) as the input. The design should include the following: *(Course Learning Outcome 5)*

i. The state diagram of the counter

[4 marks]

ii. The state transition table

[4 marks]

iii. K-maps to simplify each JK signal, and

[4 marks]

iv. Design the complete counter circuit.

[4 marks]

Question 6

a) Design MOD 8 asynchronous count up counter by using JK flip flop. The design should include the followings: *(Course Learning Outcome 5)*

i. The state transition diagram

[4 marks]

ii. K-maps to simplify each JK signal

[4 marks]

iii. Design the complete counter circuit

[4 marks]

b) Describe the main operation of 2-to-4 line decoder (active high) which has variable A and B as its input. Produce the followings: *(Course Learning Outcome 3)*

i. A complete truth table, and

[4 marks]

ii. Schematic diagram of the decoder.

[4 marks]

END OF QUESTIONS