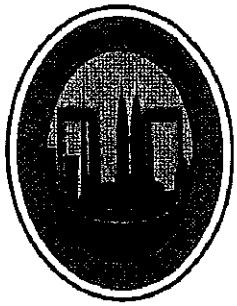

UNIVERSITI KUALA LUMPUR
MALAYSIAN INSTITUTE OF INDUSTRIAL TECHNOLOGY

FINAL EXAMINATION

JANUARY 2016 SEMESTER

COURSE CODE	:	JCB 20103
COURSE TITLE	:	DIGITAL SYSTEMS
PROGRAMME LEVEL	:	BACHELOR
DATE	:	29 MAY 2016
TIME	:	9.00 AM – 12.00 PM
DURATION	:	3 HOURS

INSTRUCTIONS TO CANDIDATES

1. Please read the instructions given in the question paper CAREFULLY.
2. This question paper is printed on both sides of the paper.
3. This question paper consists of ONE (1) section.
4. Answer FIVE (5) questions ONLY in Section A.
5. Please write your answers on the answer booklet provided.
6. Please answer all questions in English only.

THERE ARE 6 PAGES OF QUESTIONS EXCLUDING THIS PAGE.

SECTION A (Total: 100 marks)

INSTRUCTION: Answer FIVE (5) questions ONLY.
Please use the answer booklet provided.

Question 1

(a) Convert the following numbers to binary numbers:

i. $(186)_{10}$

(2 marks)

ii. $(0.2F)_{16}$

(2 marks)

iii. $(563)_{8}$

(2 marks)

(b) Perform the arithmetic operations for the following binary numbers:

i. 1001 + 101

(2 marks)

ii. 100 x 10

(2 marks)

iii. 1001 ÷ 11

(2 marks)

(c) Express the decimal number of -25 as an 8-bit number in the form of:

i. Sign magnitude.

(3 marks)

ii. 1's complement.

(2 marks)

iii. 2's complement.

(3 marks)

Question 2

(a) Determine the values of A, B, and C that make the product term $\bar{A}\bar{B}C$ equal to 1.

(3 marks)

(b) Simplify each expression below using Boolean rules;

i. $A\bar{B} + A(\overline{B+C}) + B(\overline{B+C})$

(5 marks)

ii. $\overline{AB} + \overline{AC} + \bar{A}\bar{B}\bar{C}$

(6 marks)

(c) For the following set of binary numbers, predict the output states for the below comparator.

(6 marks)

$$A_3A_2A_1A_0 = 1000, B_3B_2B_1B_0 = 1011$$

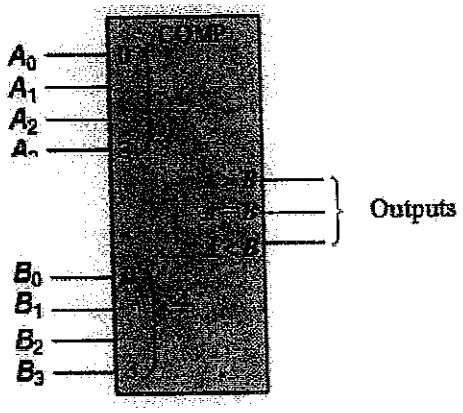

Figure 1: Comparator.

Question 3

(a) Figure 2 shows a logic gates circuit. From the figure, determine the Boolean expression. Then, simplify it using Boolean rules.

(10 marks)

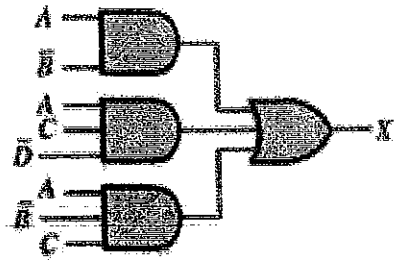

Figure 2: Logic gates circuit.

(b) Figure 3 shows a symbol of full-adder. From the figure, determine the output sum and carry out.

(4 marks)

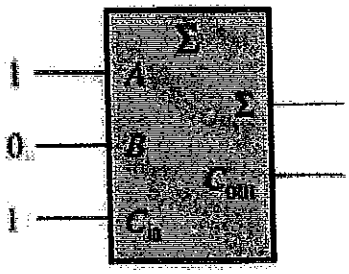

Figure 3: Full-adder.

(c) Design the logic circuit and construct a truth table represented by the following expression;

$$(A + B)(\bar{B} + C)$$

(6 marks)

Question 4

(a) Use a Karnaugh Map (K-map) to simplify the following standard SOP expression;

$$\bar{W}\bar{X}\bar{Y}\bar{Z} + W\bar{X}YZ + W\bar{X}\bar{Y}Z + \bar{W}YZ + W\bar{X}\bar{Y}\bar{Z}$$

(5 marks)

(b) For the below parallel adder, determine the completed sum by analysis of the logical operation of the circuit. Verify your result by using addition of the input numbers.

(7 marks)

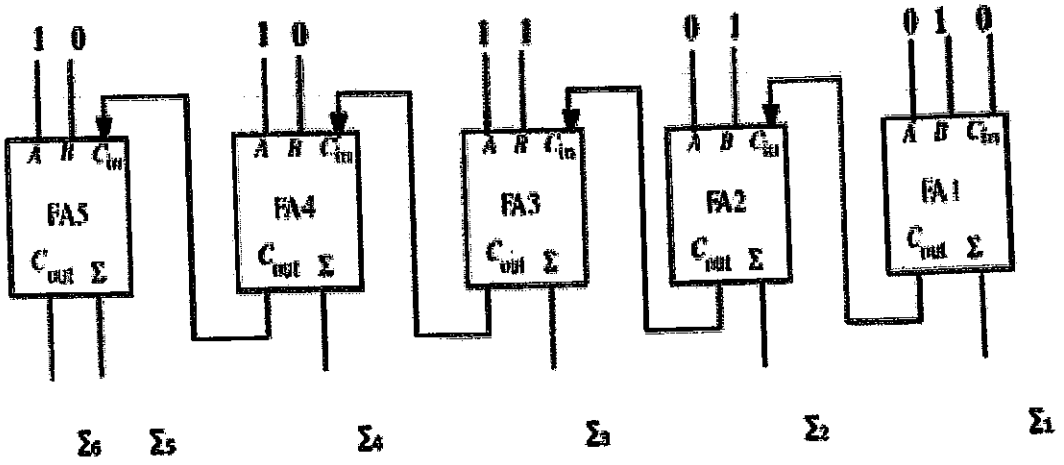

Figure 4: Parallel adder.

(c) For a gated S-R latch, analyze the Q and $\bar{Q}$ output waveform for the inputs in below figure. Show the proper relation to the enable input. Assume that Q starts LOW.

(8 marks)

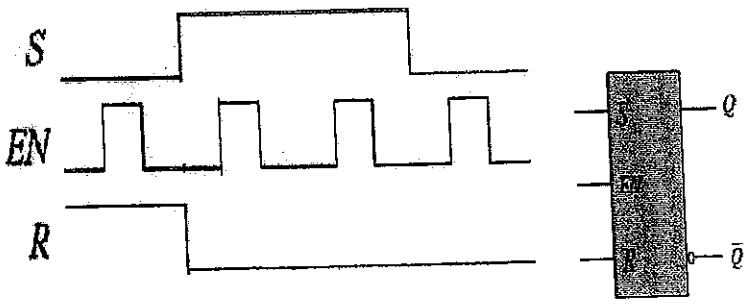

Figure 5: S-R latch waveform.

Question 5

(a) For the following Boolean expression, design the logic gates circuit.

$$A\bar{B} + A(\overline{B + C}) + B(\overline{B + C})$$

(8 marks)

(b) Assume the inputs to the 74HC42 decoders are the sequence 0001, 1010, 0111 and 0011. Describe the output.

(6 marks)

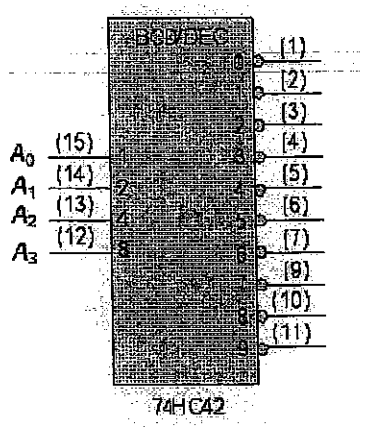

Figure 6: 74HC42 decoder.

(c) If the waveform in Figure 7 are applied to active-LOW S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume the Q starts LOW.

(6 marks)

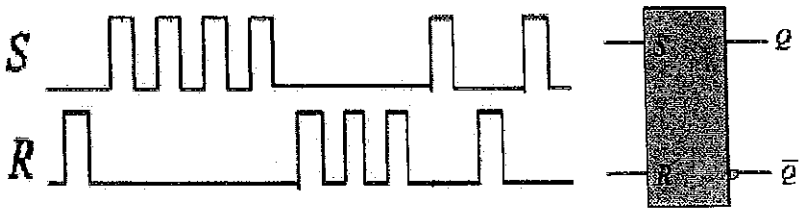

Figure 7: S-R latch waveform.

Question 6

(a) Discuss **TWO (2)** characteristics for the following modules of an XC 4000 FPGA device:

i. Switch matrix

(2 marks)

ii. Input-output block

(2 marks)

(b) Design a synchronous counter using J-K flip flops that counts the sequence of 0-1-4-5 and repeats it again.

(16 marks)

END OF EXAMINATION PAPER