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CONFIDENTIAL

SET A

UNIVERSITI KUALA LUMPUR
Malaysia France Institute

FINAL EXAMINATION

SEPTEMBER 2013 SESSION

SUBJECT CODE	:	**FLD 20403**
SUBJECT TITLE	:	**DIGITAL SYSTEM**
LEVEL	:	**DIPLOMA**
TIME / DURATION	:	**3.0 HOURS**
DATE	:	

INSTRUCTIONS TO CANDIDATES

1. **Please read the instructions given in the question paper CAREFULLY.**
2. **This question paper is printed on both sides of the paper.**
3. **Please write your answers on the answer booklet provided.**
4. **Answers should be written in blue or black ink except for sketching, graphic and illustration.**
5. **This question paper consists of TWO (2) sections. Section A and B. Answer all questions in Section A. For Section B, answer two (2) questions only.**
6. **Please answer the questions (2b), (3a), (3e) and (6b) in appendix B, and attach together with your answer booklet**
7. **Answer all questions in English.**

THERE ARE 7 PAGES OF QUESTIONS, EXCLUDING THIS PAGE AND APPENDIX.

SECTION A (Total: 60 marks)

INSTRUCTION: Answer ALL questions.
Please use the answer booklet provided.

Question 1

(a) Convert the following binary numbers to decimal number:

(i) $1101\ 1101_2$

(2 marks)

(ii) 100110.101_2

(2 marks)

(iii) 111111.111_2

(2 marks)

(b) Convert the following numbers:

(i) 111110011010.0011010_2 to Hexadecimal number

(2 marks)

(ii) $47E.5A_{16}$ to Binary number

(2 marks)

(iii) $5674.\ 342_8$ to Decimal number

(2 marks)

(c) Decode the following ASCII message.

WpN/58&@ (2 marks)

(d) Solve the following problems in 2's complement form using 8 bits.

$25_{10}\text{-}19_{10}$

(6 marks)

Question 2

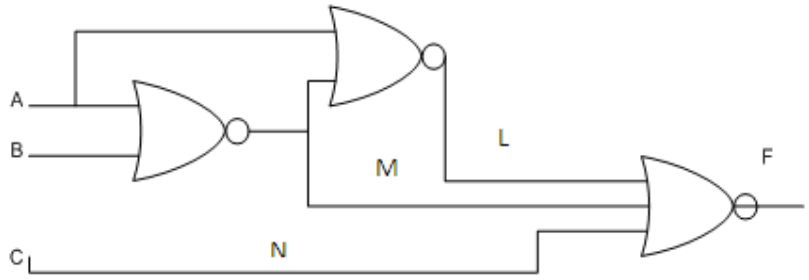


Figure 1

By referring to digital circuit in **Figure 1**, perform analysis as follows:

(a) Determine the expression of F. (5 marks)

(b) Draw the output waveform based on **Figure 2.** (Please answer this question in the **appendix B** and attach together with your answer booklet).

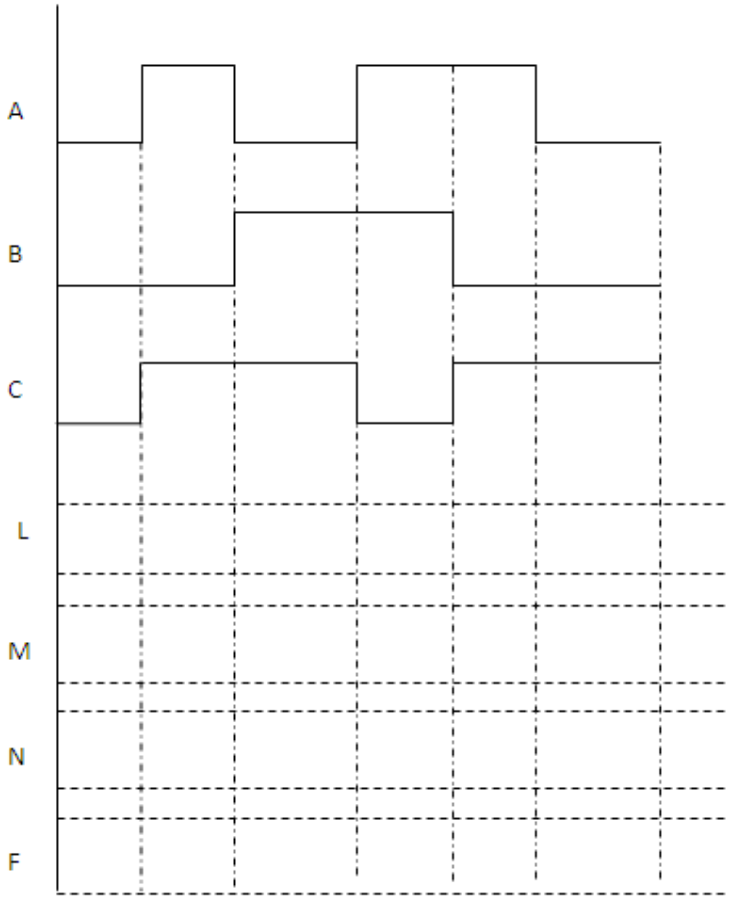


Figure 2

Question 3

(a) Give one example each for combinational logic circuit and sequential logic circuit. State the difference between combinational logic circuit and sequential logic circuit.

(2 marks)

(b) Show the logic circuit and truth table for the **S-R latch**. The truth table should consist of the input (S and R), output (Q and Q') and state of the Latch.

(4 marks)

(c) If the **S** and **R** waveforms in **Figure 3(a)** are applied to the **S-R latch**, determine the waveform that will be observed on the output, **Q, Figure 3(b)**. Assume that **Q** is initially LOW. (Please answer this question in the **appendix B** and attach together with your answer booklet).

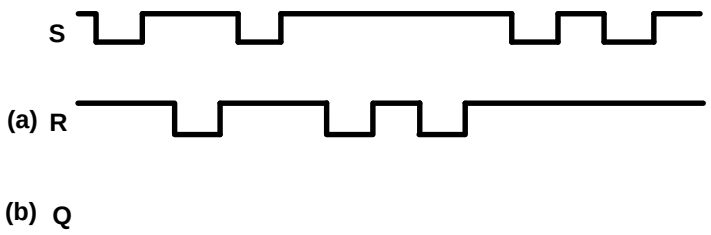


Figure 3

(4 marks)

(d) Show the logic circuit and truth table for the J-K flip-flop. The truth table should consist of the input (J and K), output $(Q)^{(t+1)}$) and state of the flip-flop.

(4 marks)

(e) If the clock (**CLK**), **J** and **K** waveforms in **Figure 4(a)** are applied to the **J-K flip-flop**, determine the waveform that will be observed on the output, **Q, Figure 4(b)**. Assume that **Q** is initially LOW. (Please answer this question in the **appendix B** and attach together with your answer booklet).

(6 marks)

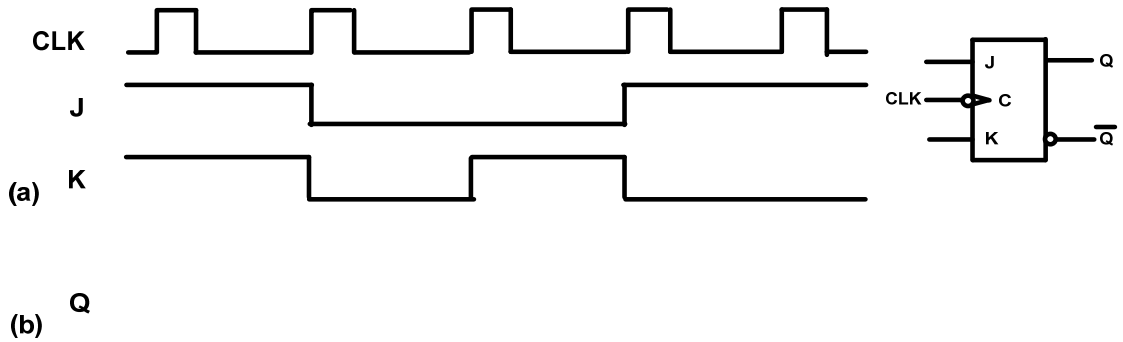


Figure 4

SECTION B (Total: 40 marks)

INSTRUCTION: Answer TWO (2) questions only

Please use the answer booklet provided.

Question 4

For the Schematic drawing in **Figure 5** below,

(a) Write Boolean expression. (4 marks)

(b) Summarize the Boolean expression of SOP form using Karnaugh map. (10 marks)

(c) Draw the simplified gates circuit. (4 marks)

(d) Replace all the gates in the simplified SOP form circuit with NAND gates. (2 marks)

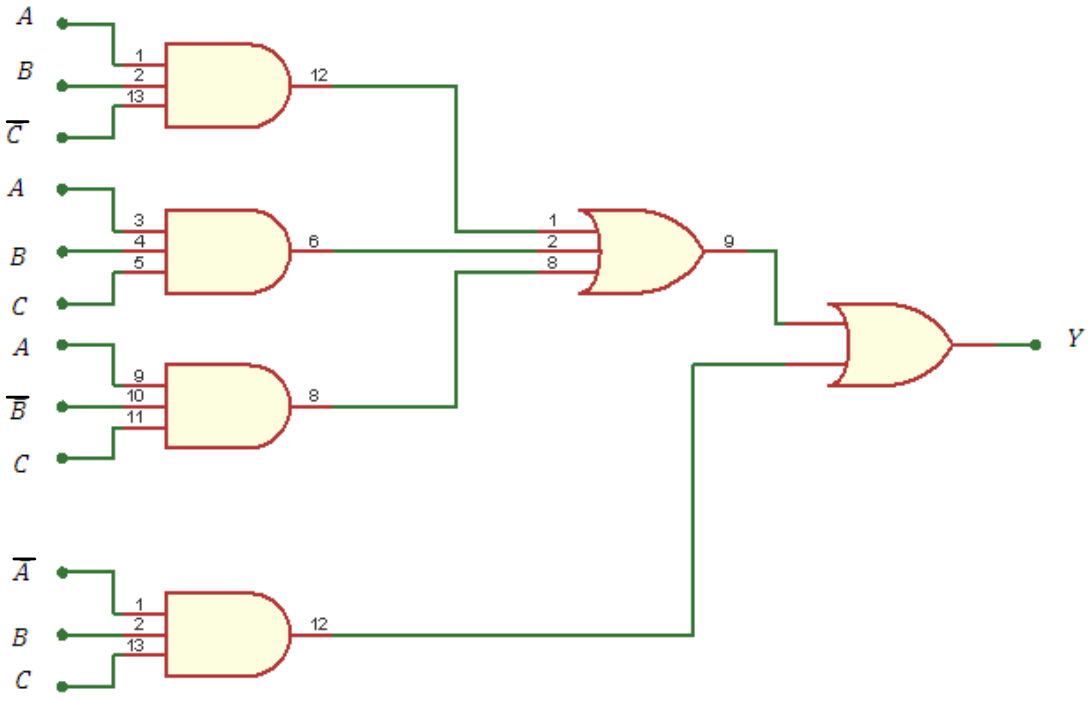


Figure 5

Question 5

(a) Design a **3 x 8 decoder** used for Binary to Octal conversion by showing the following steps.

(i) Truth Table

(4 marks)

(ii) Logic circuit

(3 marks)

(iii) Output expressions

(3 marks)

(b) Implement the following Boolean functions with two **2 x 4 decoders** and a **1 x 2 decoder**.

F1 (A, B, C) =∑m (2, 3, 6, 7)

(4 marks)

(c) Design a **4 to 1 Multiplexer**. The design should include the following;

(i) Block diagram

(2 marks)

(ii) Truth table

(2 marks)

(iii) Logic circuit

(2 marks)

Question 6

(a) List the difference between synchronous and asynchronous counters.

(2 marks)

(b) Refer to block diagram in **Figure 6**:

(i) Identify the modulus and the counter type.

(4 marks)

(ii) Draw the complete timing diagram for sixteen clock pulses for the counter in part (i), showing the output waveform for $\mathbf{Q_0}$, $\mathbf{Q_1}$ and $\mathbf{Q_2}$.

(14 marks)

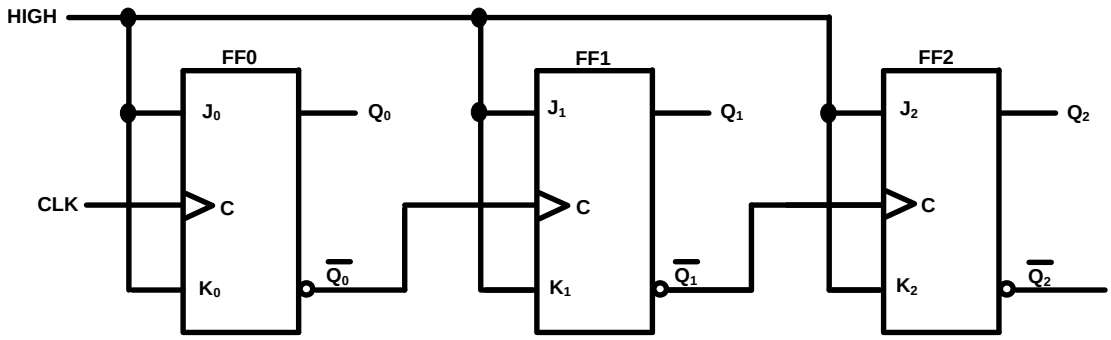


Figure 6

END OF QUESTION PAPER

APPENDIX A

BOOLEAN THEOREMS

1. $X \bullet 0 = 0$
2. $X \bullet 1 = X$
3. $X \bullet X = X$
4. $X \bullet \overline{X} = 0$
5. $X + 0 = X$
6. $X + 1 = 1$
7. $X + X = X$
8. $X + \overline{X} = 1$
9. $X + Y = Y + X$
10. $X \bullet Y = Y \bullet X$
11. $X + (Y + Z) = (X + Y) + Z = X + Y + Z$
12. $X(YZ) = (XY)Z = XYZ$

13a. $X(Y + Z) = XY + XZ$

13b. $(W + X)(Y + Z) = WY + XY + WZ + XZ$

14. $X + XY = X$
15. $X + \overline{X}Y = X + Y$
16. $\overline{X + Y} = \overline{X}\,\overline{Y}$
17. $\overline{XY} = \overline{X} + \overline{Y}$
18. $\overline{\overline{A}} = A$

ASCII table:

	MSBs							
LSBs	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
0000	NUL	DLE	SP	0	@	P	`	p
0001	SOH	DC_1	!	1	A	Q	a	q
0010	STX	DC_2	"	2	B	R	b	r
0011	ETX	DC_3	#	3	C	S	c	s
0100	EOT	DC_4	$	4	D	T	d	t
0101	ENQ	NAK	%	5	E	U	e	u
0110	ACK	SYN	&	6	F	V	f	v
0111	BEL	ETB	'	7	G	W	g	w
1000	BS	CAN	(	8	H	X	h	x
1001	HT	EM	)	9	I	Y	i	y
1010	LF	SUB	*	:	J	Z	j	z
1011	VT	ESC	+	;	K	[	k	{
1100	FF	FS	,	<	L	\	l	|
1101	CR	GS	-	=	M	]	m	}
1110	O	RS	.	>	N	^	n	~
1111	SI	US	/	?	O	_	o	DEL

APPENDIX B

Name:_____

ID NO:_____

CODE/SUBJECT:_____

LECTURER:_____

Question (2b)

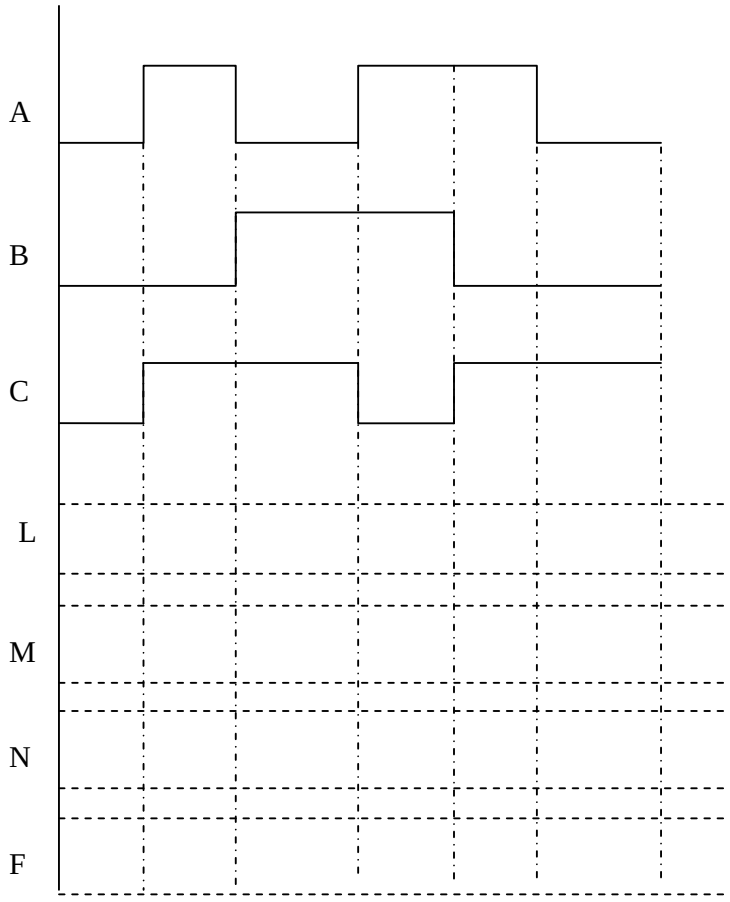


Figure 2

Question (3c)

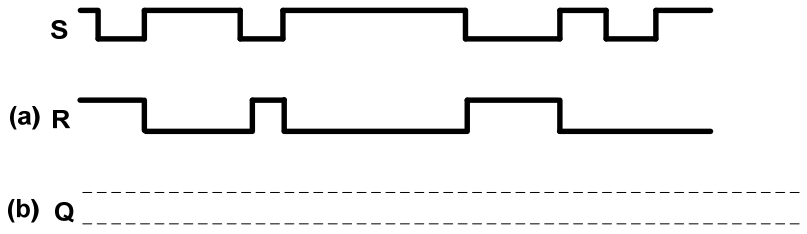


Figure 3

Question (3e)

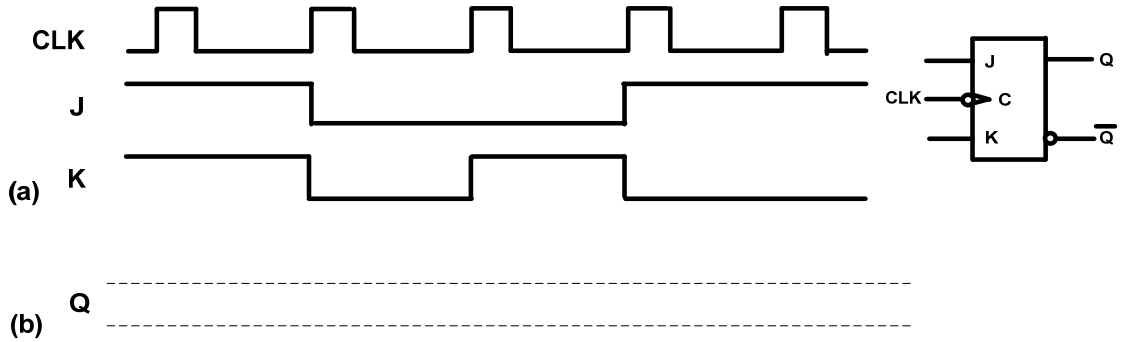


Figure 4

Question (6b)

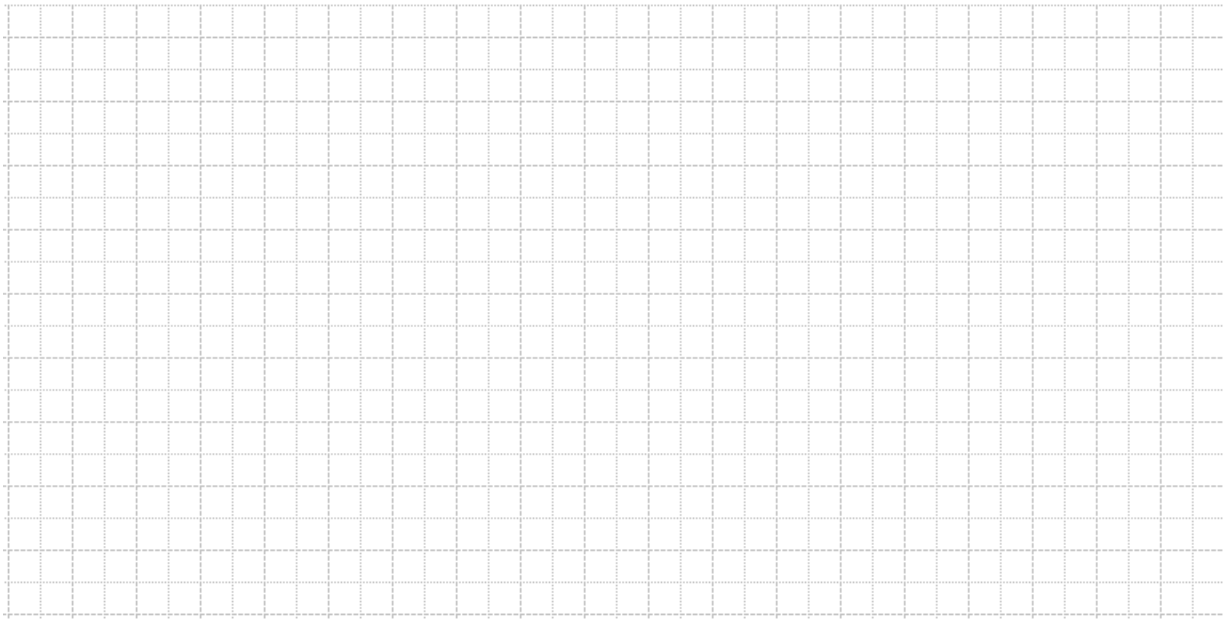


Figure 6

Answers

Question (3c)

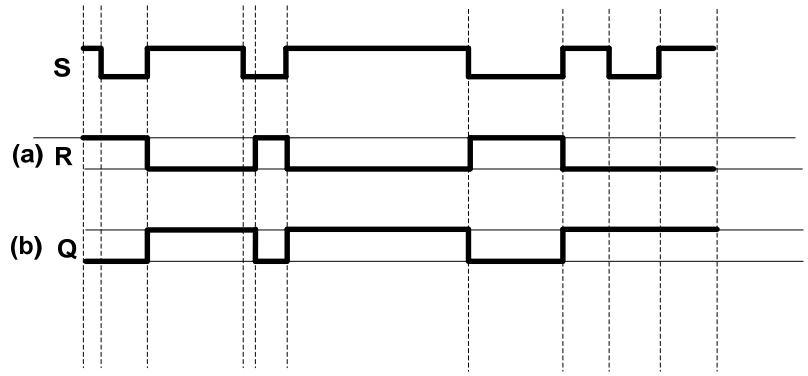


Figure 3

Question (3e)

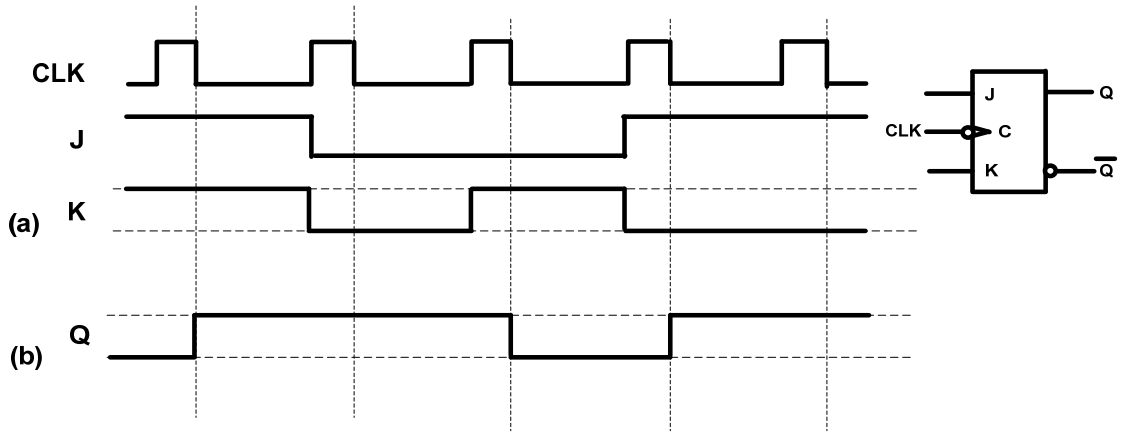


Figure 4

Part B

(Q5)

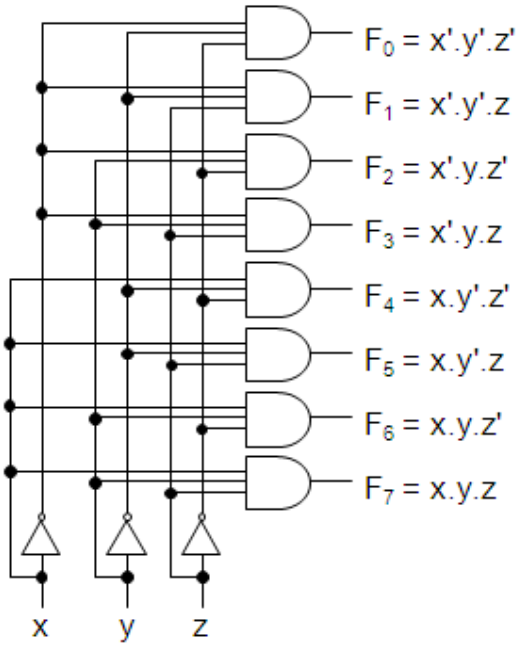
(a)(i)

- Design a 3×8 decoder.

x	y	z	F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

(4 marks)

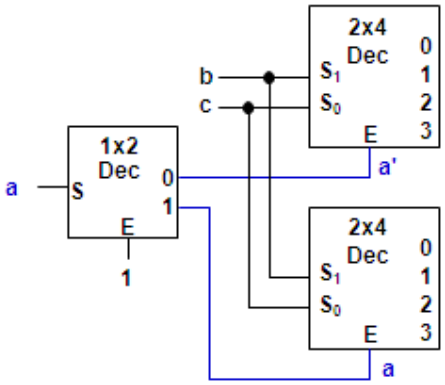
(ii and iii)



Logic circuit (4 marks)
Logic expression (4 marks)

(5b) Implement the following Boolean functions with a **1 x 2 decoders and** two **2 x 4 decoder**.

F1 (A, B, C) =∑m (2, 3, 6, 7)

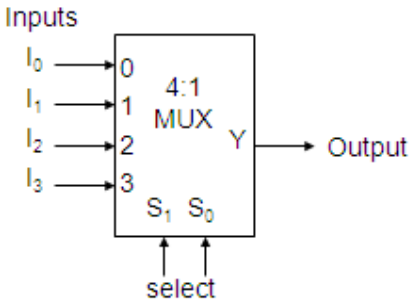


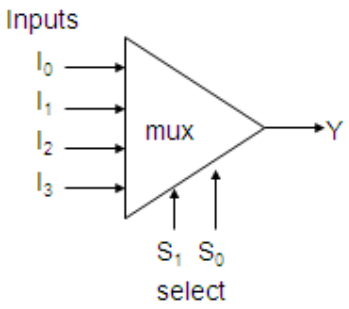
(Q6) Design a **4 to 1 Multiplexer**

- Truth table for a 4-to-1 multiplexer:

I_0	I_1	I_2	I_3	S_1	S_0	Y
d_0	d_1	d_2	d_3	0	0	d_0
d_0	d_1	d_2	d_3	0	1	d_1
d_0	d_1	d_2	d_3	1	0	d_2
d_0	d_1	d_2	d_3	1	1	d_3

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3





Q6(b)

(i) **The synchronous counter:** all flip-flops in the counter is clocked at the same time by a common clock pulse; but

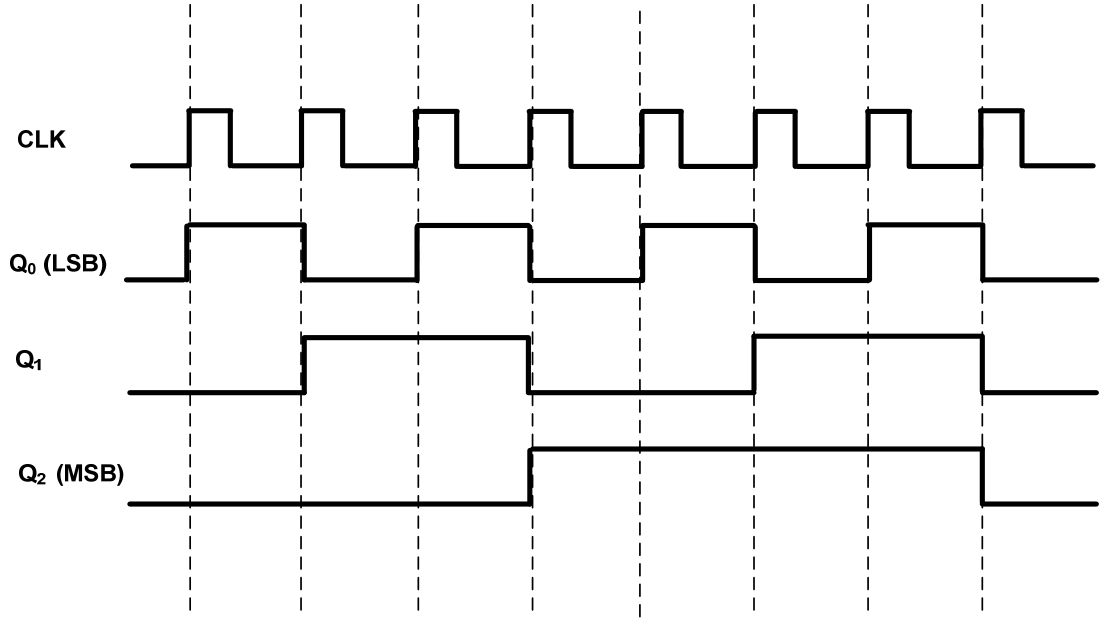
The asynchronous counter: the flip-flop within the counter do not change at the same time because they do not have a common clock pulse.

(2 marks)

(ii) Modulus 8 (2 marks)

Asynchronous counter (2 marks)

(ii)



(14 marks)