Document No : UniKL MFI_SD_AC41
Revision No: 02
Effective Date: 01 December 2008

CONFIDENTIAL

SET A

UNIVERSITI KUALA LUMPUR
Malaysia France Institute

FINAL EXAMINATION

SEPTEMBER 2013 SESSION

SUBJECT CODE	:	**FLB 23043**
SUBJECT TITLE	:	**DIGITAL SYSTEM**
LEVEL	:	**BACHELOR**
TIME / DURATION	:	**2.5 HOURS**
DATE	:	

INSTRUCTIONS TO CANDIDATES

1. **Please read the instructions given in the question paper CAREFULLY.**
2. **This question paper is printed on both sides of the paper.**
3. **Please write your answers on the answer booklet provided.**
4. **Answers should be written in blue or black ink except for sketching, graphic and illustration.**
5. **This question paper consists of TWO (2) sections. Section A and B. Answer all questions in Section A. For Section B, answer two (2) questions only.**
6. **Answer all questions in English.**

THERE ARE 6 PAGES OF QUESTIONS, EXCLUDING THIS PAGE AND APPENDIX.

SECTION A (Total: 40 marks)

INSTRUCTION: Answer ALL questions.
Please use the answer booklet provided.

Question 1

(a) Each of the following numbers is a signed binary number in the 2's complement system. Determine the decimal value for each case.

i. 01101 (2 marks)
ii. 10110 (3 marks)
iii. 10011 (3 marks)

(b) Perform addition of the following decimal numbers in BCD system.

i. 59_{10} and 38_{10} (3 marks)

ii. 135_{10} and 265_{10} (4 marks)

Question 2

Determine the Boolean expression at output H and simplify the expression using Boolean's rules and laws and De Morgan theorem for **Figure 1**.

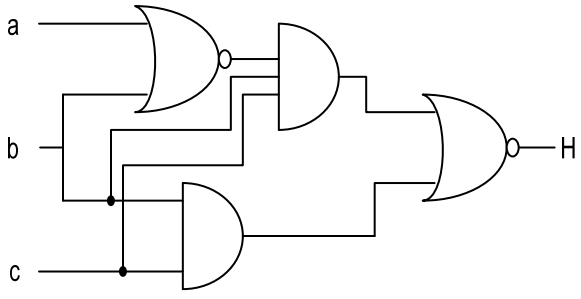

Figure 1

(6 marks)

Question 3

Using Karnaugh maps, obtain a minimum simplified expression for the following Boolean function in sum of products (SOP) form. Then draw the minimum simplified logic circuit for the simplified expression.

i. $Z = \overline{A}\overline{B}CD + \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D + \overline{A}BCD + AB\overline{C}D + ABCD + A\overline{B}CD$

(5 marks)

ii. $Y(A, B, C, D) = \sum(1, 3, 4, 6, 8, 9, 11, 13, 14)$

(7 marks)

Question 4

Implement the following Boolean function with an **8 x 1 multiplexer**. Choose variable **A** as an input to 8 x 1 multiplexer. Give the truth table and circuit connection for 8 to 1 multiplexer.

F1 (A, B, C, D) = ∑m (1, 2, 5, 7, 9, 11, 14)

(7 marks)

SECTION B (Total: 60 marks)

INSTRUCTION: Answer TWO (2) questions only

Please use the answer booklet provided.

Question 5

(a) Simplify the logic circuit shown in **Figure 2** by performing the following steps.

i. Simplify the output expression, z (8 marks)

ii. Draw a logic circuit for simplified expression, z (2 marks)

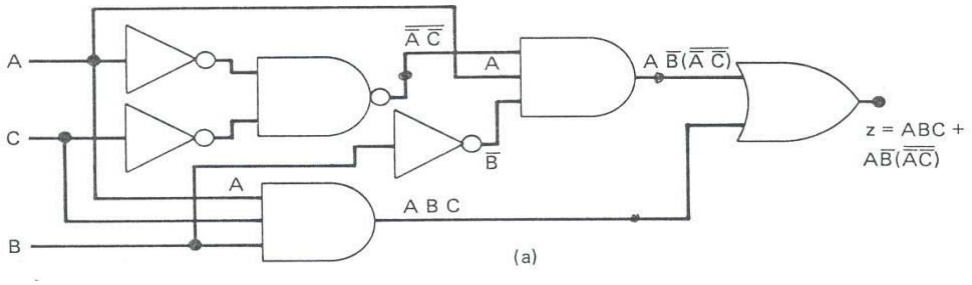

Figure 2

(b) The Apex Corporation chemical processing plant uses a computer to monitor the temperature and pressure of four chemical tanks, as shown in **Figure 3(a)**. Whenever a temperature or a pressure exceeds the danger limit, an internal tank sensor applies a '1' to its corresponding output to the computer. If all conditions are OK, then all outputs are '0'. Layout of binary data read by the computer monitoring system is shown in **Figure 3(b)**.

i. If the computer reads the binary string 0010 1000, what problems exist?

(4 Marks)

ii. What problem exist if the computer is reading 55H (55 hex)?

(4 Marks)

iii. What hexadecimal number is read by the computer if the temperature and pressure in both tanks D and B are high?

(4 Marks)

iv. Tanks A and B are taken out of use and their sensor outputs are connected to 1's. A computer programmer must write a program to ignore these new circuit conditions. The computer program must check that the value read is always less than what decimal equivalent when no problem exists?

(4 Marks)

v. In another area of the plant, only three tanks (A, B, and C) have to be monitored. What octal number is read if tank B has a high temperature and pressure?

(4 Marks)

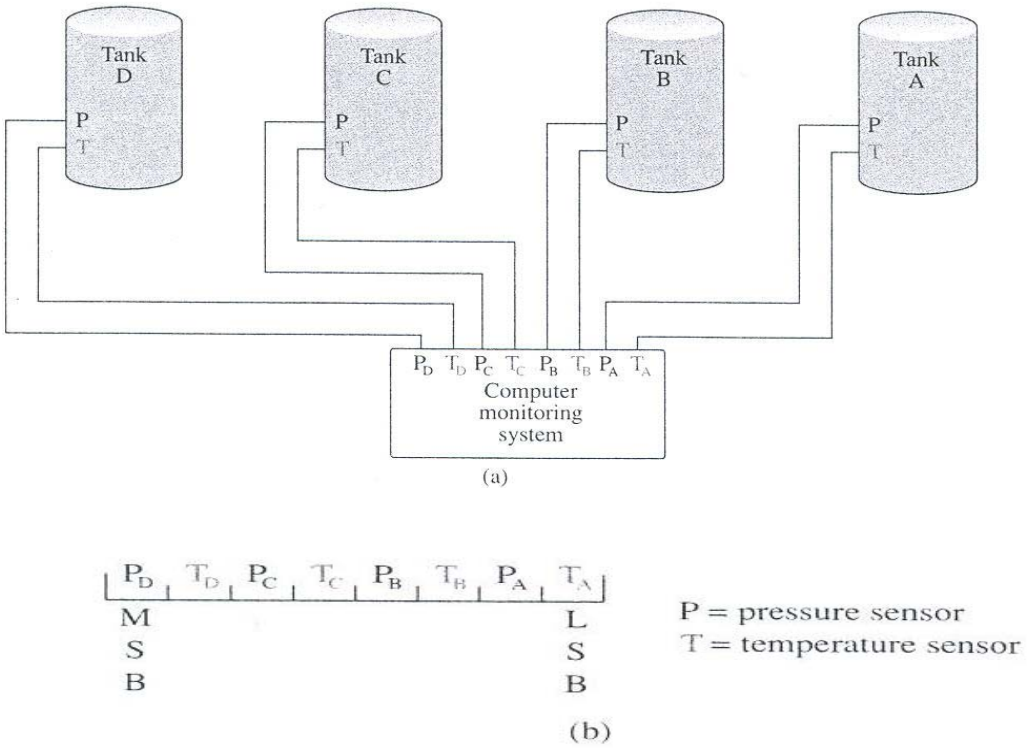

Figure 3(a) and 3(b)

Question 6

(a) Design a 3 x 8 decoder used for Binary to Octal conversion by showing the following steps.

i. Truth Table (4 marks)

ii. Logic circuit (3 marks)

iii. Output expressions (8 marks)

(b) Consider a active-High S-R Latch, has the following input sequences,
Set = **1001 0101** and Reset = **1010 1101**

Predict the output pair, Q and Q' for each pair of the input sequences, assume initial value for Q = 0. For each output, write the Latch state whether Set, Reset, No change or Invalid.

Your answer should have the following:

i. S-R logic circuit

(2 marks)

ii. Truth Table consists of the input (S and R), output (Q and Q') and state of the Latch.

(13 marks)

Question 7

a) For counter in **Figure 4**, answer the following questions;

i. Determine the MOD number of the counter.

(6 marks)

ii. Determine the frequency at the D output.

(3 marks)

iii. Construct a MOD-10 counter by showing its gates connection. This counter needs to count from 000 through 1001.

(8 marks)

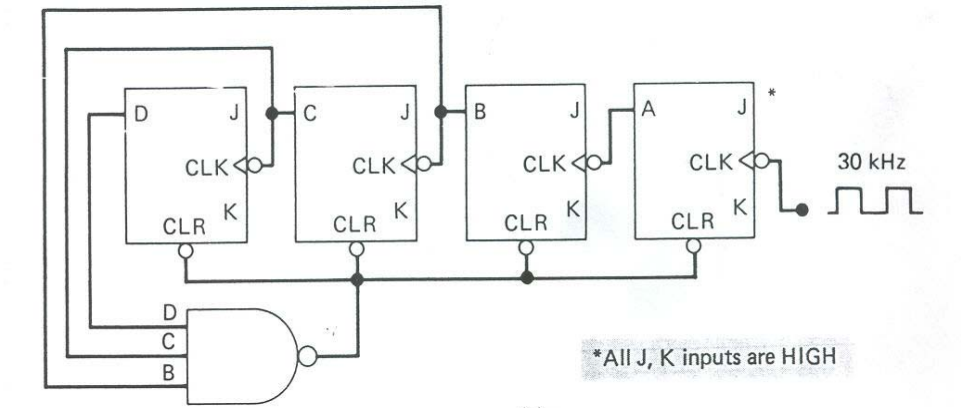

Figure 4

b) The first step involved in building a digital clock is to take the 60 Hz power line waveform and feed it into a shaping circuit to produce a square wave as shown in **Figure 5**. The 60 Hz square wave is then put into a MOD-60 counter, which is used to divide the 60 Hz frequency by exactly 60 to produce a 1-Hz waveform. This 1-Hz waveform is fed to series of counters, which then count seconds, minutes, hours, and so on.

i. How many FFs are required for the MOD-60 counter?

(5 marks)

ii. This MOD-60 counter was needed to divide the 60-Hz line frequency down to 1Hz. Construct an appropriate MOD-60 counter by showing its gates connection.

(8 marks)

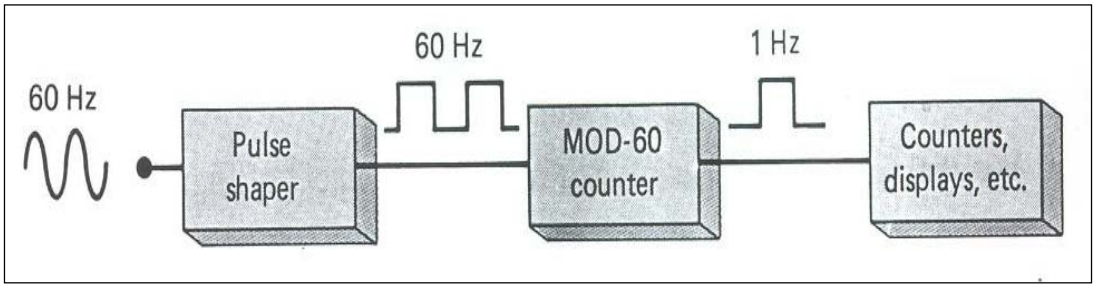

Figure 5

END OF QUESTION PAPER

APPENDIX

BOOLEAN THEOREMS

1. $X \bullet 0 = 0$
2. $X \bullet 1 = X$
3. $X \bullet X = X$
4. $X \bullet \overline{X} = 0$
5. $X + 0 = X$
6. $X + 1 = 1$
7. $X + X = X$
8. $X + \overline{X} = 1$
9. $X + Y = Y + X$
10. $X \bullet Y = Y \bullet X$
11. $X + (Y + Z) = (X + Y) + Z = X + Y + Z$
12. $X(YZ) = (XY)Z = XYZ$

13*a*. $X(Y + Z) = XY + XZ$

13*b*. $(W + X)(Y + Z) = WY + XY + WZ + XZ$

14. $X + XY = X$
15. $X + \overline{X}Y = X + Y$
16. $\overline{X + Y} = \overline{X}\,\overline{Y}$
17. $\overline{XY} = \overline{X} + \overline{Y}$
18. $\overline{\overline{A}} = A$