SET B

UNIVERSITI KUALA LUMPUR
Malaysia France Institute

FINAL EXAMINATION
JULY 2010 SESSION

SUBJECT CODE	:	FLB 20203
SUBJECT TITLE	:	DIGITAL SYSTEM
LEVEL	:	BACHELOR
TIME / DURATION	:	9.00 am – 12.00 noon (3 HOURS)
DATE	:	14 NOVEMBER 2010

INSTRUCTIONS TO CANDIDATES

1. Please read the instructions given in the question paper CAREFULLY.

2. This question paper is printed on both sides of the paper.

3. Please write your answers on the answer booklet provided.

4. Answer should be written in blue or black ink except for sketching, graphic and illustration.

5. This question paper consists of TWO (2) sections. Section A and B. Answer all questions in Section A. For Section B, answer two (2) question only.

6. Answer all questions in English.

THERE ARE 6 PAGES OF QUESTIONS, EXCLUDING THIS PAGE.

SECTION B (Total: 60 marks)

INSTRUCTION: Answer only TWO (2) questions.
Please use the answer booklet provided.

Question 5

(a) Design a MOD- 6 up asynchronous counter using JK flip-flop with NGT clock. The
design should include the following:

    (i)   Counting sequence   (5 marks)

    (ii)   Circuit diagram.   (5 marks)

(b) Design a synchronous counter using JK flip-flop with sequence as shown in the state
diagram of Figure 1. The design should include the following:

    (i)   Excitation table   (5marks)
    (ii)   Karnaugh map   (5 marks)
    (iii)   Circuit diagram   (10 marks)
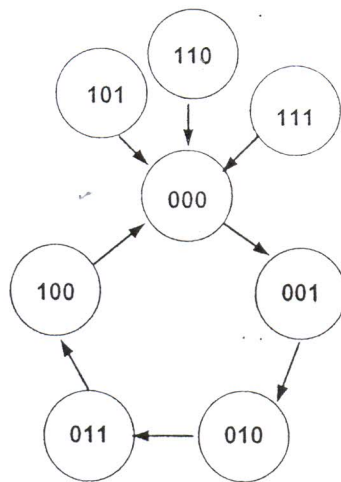

Figure 1

Question 6

In an electronic equipments refurbishment project, there is an engineering task whereby an old digital PCB using TTL technology is to be integrated into a new PCB incorporating other new design circuitry. To reduce parts count, unnecessary wiring and to increase reliability, a certain logic performed by the circuitry in *Figure* 2 below is required to be replaced by a single CMOS IC multiplexer. A multiplexer allows decoding of certain logic by using its data and select inputs.

(a)   From the logic circuit in FIGURE 1, obtain its simple Boolean expression. Develop and expand the Boolean equation in standard S.O.P form, F= (W,X,Y,Z).

(8 marks)

(b)   Deduce its complete minterm expression.

(5 marks)

(c)   Fill in the Karnaugh map accordingly.

(2 marks)

(d)   One of the advantages of using multiplexer design is to be able to decode 4 variables logic with only 3 select variables. Provide the corresponding truth table with W, X, and Y as the select inputs by analyzing the Karnaugh map. (Hint: Construct a truth table with only W, X, Y as inputs. The output is only F. Fill in F with 0, 1 or Z or Z'. Perform analysis for each case of W,X,Y on the Karnaugh map. You can start with W,X,Y = 0,0,0 which resultant F can be 0,1,Z or Z').

(10 marks)

(e)   Draw the resultant multiplexer diagram.
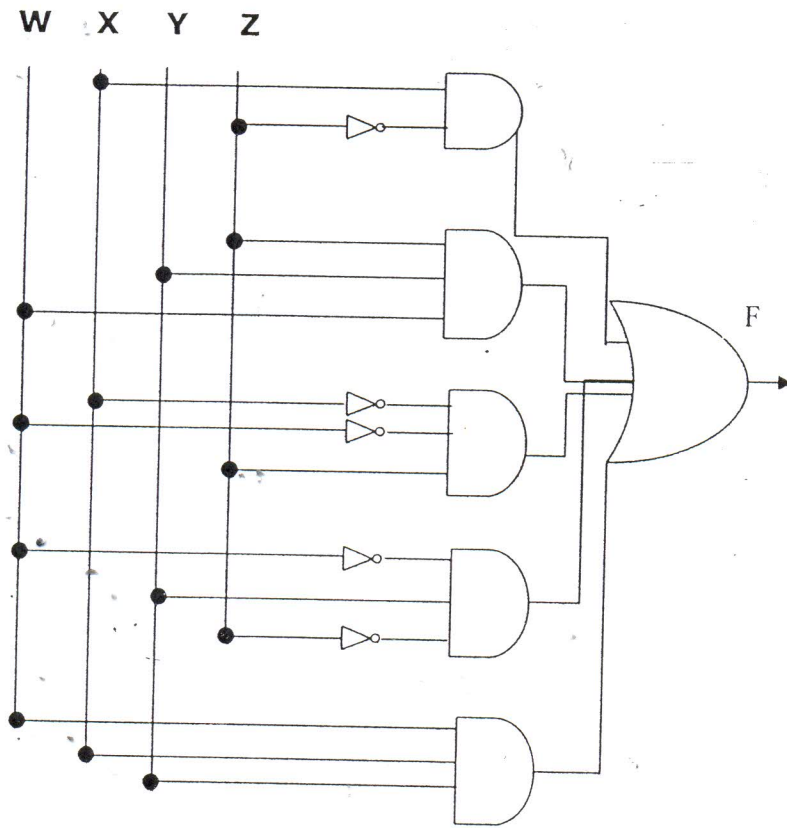
(5 marks)

Figure 2

Question 7

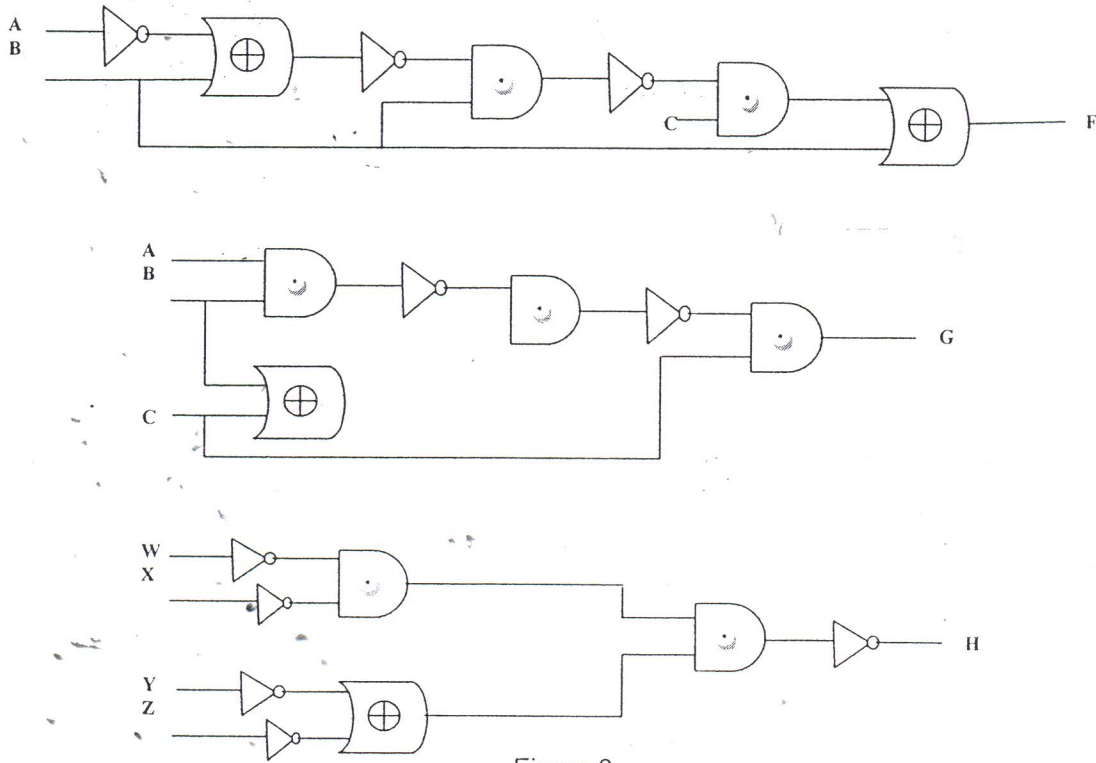Refer to Figure 3.

Figure 3

(a)   Find F, G and H. Also simplify them.   (6 marks)

(b)   Calculate Minterm and Maxterm of functions.   (12 marks)

(c)   Minimize Minterm values by using Karnaugh Map.   (12 marks)

END OF QUESTION PAPER