CONFIDENTIAL

SET B



UNIVERSITI KUALA LUMPUR

MALAYSIA FRANCE INSTITUTE

FINAL EXAMINATION JANUARY 2011 SEMESTER

SUBJECT CODE

: FLD 20402

SUBJECT TITLE

: DIGITAL SYSTEM

LEVEL

: DIPLOMA

DURATION

: 12.30pm - 2.30pm

(2 HOURS)

DATE / TIME

: 10 MAY 2011

INSTRUCTIONS TO CANDIDATES

- 1. Please read the instructions given in the question paper CAREFULLY.
- 2. This question paper is printed on both sides of the paper.
- 3. Please write your answers on the answer booklet provided.
- 4. Answers should be written in blue or black ink except for sketching, graphic and illustration.
- 5. This question paper consists of TWO (2) sections. Section A and B. Answer all questions in Section A. For Section B, answer two (2) questions only.
- 6. Answer all questions in English.

THERE ARE 7 PRINTED PAGES OF QUESTIONS, EXCLUDING THIS PAGE.

SECTION A (Total: 60 marks)

INSTRUCTION: Answer ALL questions.
Please use the answer booklet provided.

Question 1

- (a) Convert the following numbers of different number system into the stated number system (show your step of conversion):
 - i. 175₈ to decimal number

(2 marks)

ii. 1063₈ to binary number

(2 marks)

iii. 2597₈ to BCD number

(2 marks)

iv. 9CAF₁₆ to Binary and Octal number

(4 marks)

v. 1011011001100111₂ to Octal and Hexadecimal number.

(4 marks)

vi. 23456₁₀ to Binary, Octal and Hexadecimal number.

(6 marks)

- (a) Draw the logic gate and its truth table for the gates below:
 - i. 2 input Exclusive-NOR (Ex-NOR) gate

(3 marks)

ii. 3 input NAND gate

(3 marks)

- (b) Figure 1 shows the combinational logic gates with 3 input variables A, B and C.
 - i. Determine the Boolean Equation for the output X.

(2 marks)

ii. Simplify the Boolean Equation either using Karnaugh Mapping procedure or Boolean reduction for the output X.

(3 marks)

iii. Draw the simplified logic circuit.

(3 marks)

iv. Determine the output waveform for X in Figure 2.

(6 marks)

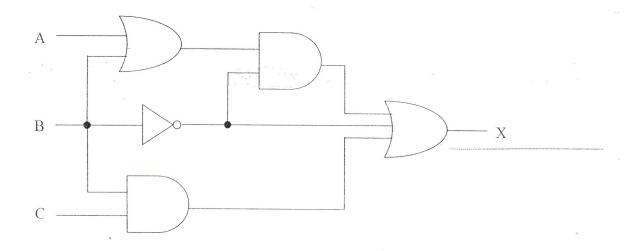


Figure 1

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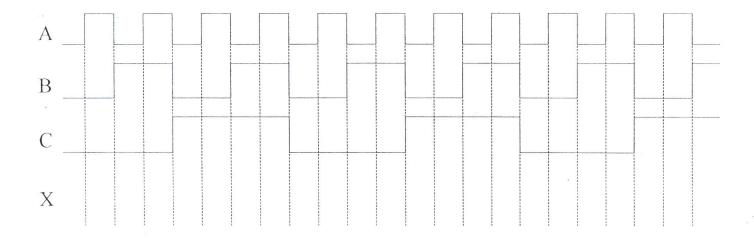


Figure 2

Figure 3 shows two T type flip Flops.

(a) Draw the truth table of this flip flop.

(3 marks)

(b) Construct the flip flop using NANDs gate.

(5 marks)

(c) State the main function of this flip flop.

(2 marks)

(d) Determine the output waveform of QA.

(5 marks)

(e) Determine the output waveform of QB.

(5 marks)

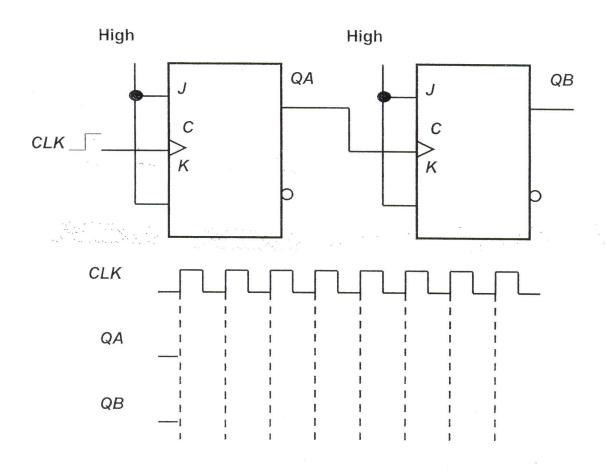


Figure 3

SECTION B (Total: 40 marks)

INSTRUCTION: Answer TWO (2) questions only

Please use the answer booklet provided.

Question 4

Design a half adder;

(a) Construct the truth table

(6 marks)

(b) Indicate the sum-of-product expressions

(4 marks)

(c) Determine the Karnaugh Map

(6 marks)

(d) Draw the circuit.

(4 marks)

Figure 4 shows a chemical plant system that needs a microprocessor-driven alarm system to warn of critical condition in one of its chemical tanks. The tank has four switches that monitor temperature (T), pressure (P), fluid level (L), and weight (W). **Table 1** shows the conditions that will notify the microprocessor to activate an alarm when any of the following conditions arise.

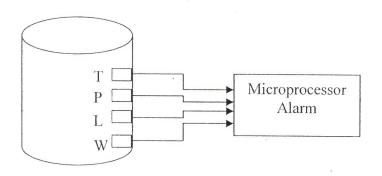


Figure 4

Table 1

CONDITION	Temperature (T)	Pressure (P)	Fluid level (L)	Weight (W)
- 1	HIGH	HIGH	HIGH	don't care
2	· HIGH	don't care	LOW	HIGH
3	LOW	HIGH	LOW	don't care
4	HIGH	don't care	LOW	LOW

(a) Determine the Boolean equation to activate the alarm system.

(5 marks)

(b) Simplify the Boolean equation using Karnaugh Map

(5 marks)

(c) Simplify the Boolean equation using Boolean algebra.

(5 marks)

(d) Draw the simplify logic gate circuit.

(5 marks)

Figure 5 shows a counter circuit.

(a) Define a positive edge triggered clock and a negative edge triggered clock.

(2 marks)

(b) Determine the type of this counter.

(2 marks)

(c) Determine the sequence of states in a truth table.

(5 marks)

(d) Draw the complete timing diagram for 8 clock pulses.

(5 marks)

(e) Modify this circuit, so that the switch up-counter can control the count from 0-1-2-3-4-5-6-0-1-2-3-4-5-6 and so on.

(6 marks)

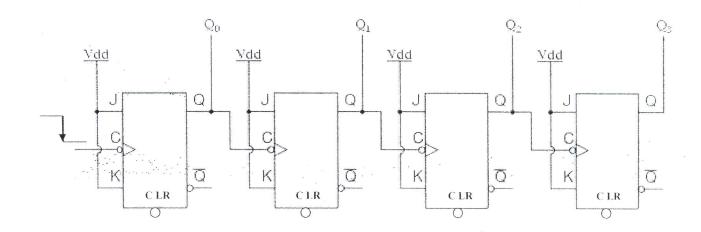


Figure 5

END OF QUESTION PAPER