UNIVERSITI KUALA LUMPUR
MALAYSIAN INSTITUTE OF MARINE ENGINEERING TECHNOLOGY

FINAL EXAMINATION
JANUARY 2017 SEMESTER

COURSE CODE	: LEB10202
COURSE NAME	: MARINE ELECTRONICS
PROGRAMME NAME (FOR MPU: PROGRAMME LEVEL)	: BACHELOR OF ENGINEERING TECHNOLOGY (HONS) IN NAVAL ARCHITECTURE & SHIPBUILDING
DATE	: 04/07/2017 TUE
TIME	: 2.00 PM - 04.00 PM
DURATION	: 2 HOURS

INSTRUCTIONS TO CANDIDATES

1. Please read CAREFULLY the instructions given in the question paper.
2. This question paper has information printed on both sides.
3. This question paper consists of FIVE (5) questions. Answer FOUR (4) questions only.
4. Please write yours answers on the answer booklet provided.
5. Write your answers only in BLACK or BLUE ink.
6. Answer all questions in English.

THERE ARE 7 PAGES OF QUESTIONS, EXCLUDING THIS PAGE.

INSTRUCTION: Answer any FOUR (4) questions only.
Please use the answer booklet provided.

Question 1(CLO 1 & CLO 2)

(a) Apply De-Morgan's theorem to each expression:

i. $\overline{A\bar{B}(C+D)}$

(2 marks)

ii. $\overline{\mathrm{RST}}\,\overline{(\mathrm{R}+\mathrm{S}+\mathrm{T})}$

(2 marks)

ii. $\overline{\overline{\overline{\overline{(A+B)}\overline{(C+D)}}\overline{(E+F)}}\overline{(G+H)}}$

(2 marks)

(b) Based on Figure Q1 (b) below,

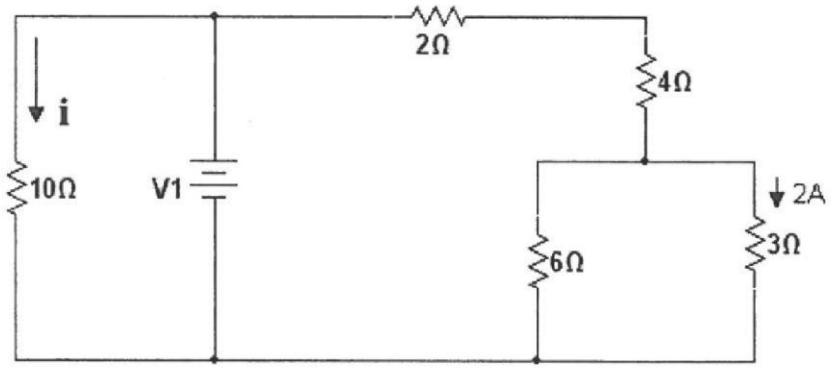

Figure Q1 (b)

i. Identify the passive and active elements.

(2 marks)

ii. Determine the number of branches and nodes.

(3 marks)

iii. Calculate the value of i.

(8 marks)

iv. Calculate the V1 value.

(6 marks)

Question 2(CLO 1 & CLO 2)

(a) For the circuit shown in Figure Q2 (a), below

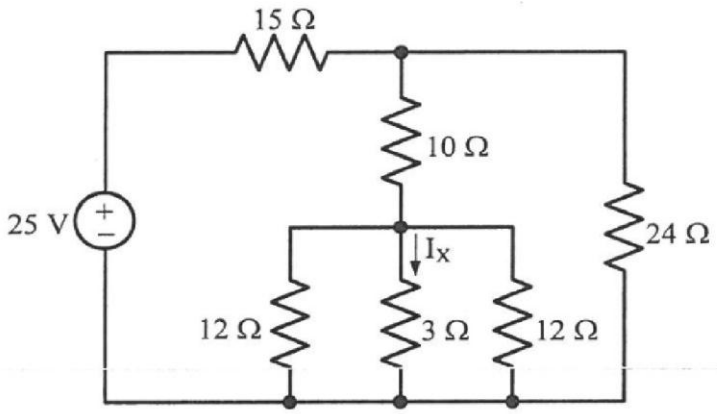

Figure Q2 (a)

i. Calculate the equivalent resistance. (3 marks)

ii. Determine the value of Ix. (7 marks)

(b) Calculate the output voltage for the adder circuit shown in Figure Q2 (b) below, if Rs1=Rs2=Rs3=1kΩ and Rf=10kΩ.

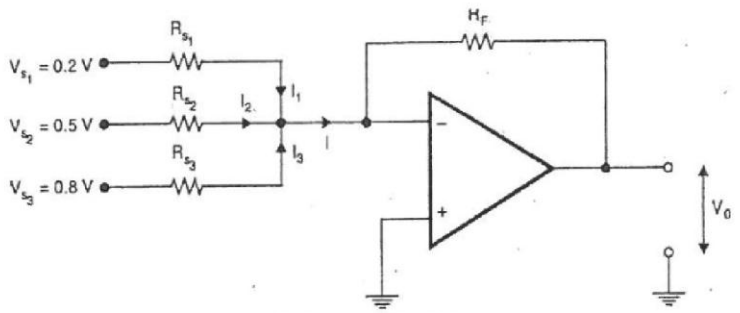

Figure Q2 (b)

(3 marks)

(c) For the Table Q2(c) below,

	CD			
AB	1	1	1	1
	1	1	0	0
	0	0	0	1
	0	0	1	1

Table Q2(c)

i. Determine the minimum expression in Table Q2 (c) by using K-Map.

(3 marks)

ii. Draw the logic diagram for the answer in Question 2(c) (i).

(5 marks)

(d) For a PN junction, draw and label each of the components a for applying:

i. Forward bias.

(2 marks)

ii. Reverse bias.

(2 marks)

Question 3(CLO 1 & CLO 2)

(a) Explain the differences between intrinsic and extrinsic material.

(4 marks)

(b) For the circuit as shown in Figure Q3(b),

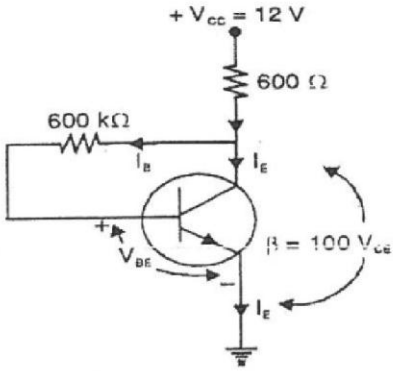

Figure Q3(b)

i. Determine the emitter current by neglecting V_{BE}.

(8 marks)

ii. Calculate V_{CE}.

(3 marks)

(c) Derive the input-output relationship for the differential amplifier circuit in Figure Q3 (c) below.

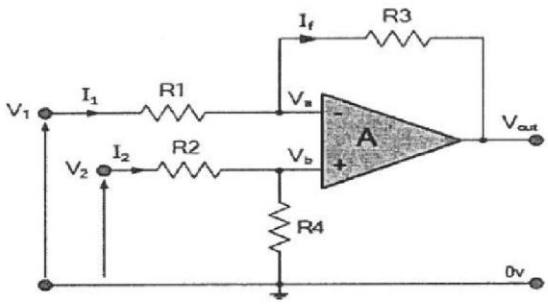

Figure Q3 (c)

(10 marks)

Question 4(CLO 1 & CLO 2)

(a) Perform the subtraction operation on these numbers using 1's and 2's complement method.

i. 148_{10}-78_{10}

(2 marks)

ii. 29_{10}-93_{10}

(2 marks)

(b) Calculate the total capacitance value at the terminals a and b for a circuit shown in Figure Q4 (a) below.

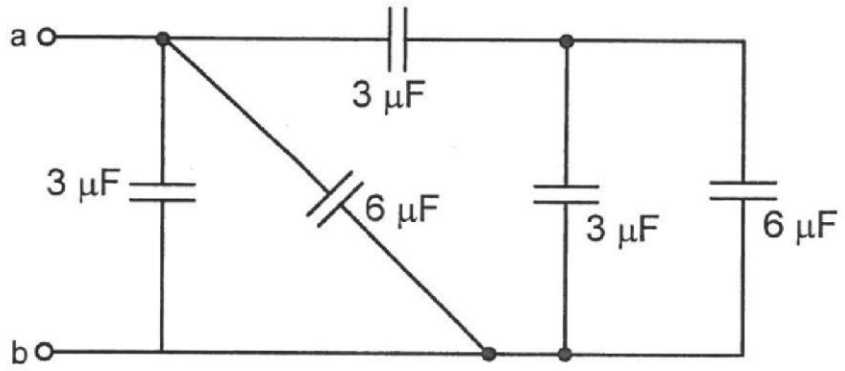

Figure Q4(b)

(3 marks)

(c) For the inverting amplifier shown in Figure Q4 (c) below, determine the range of the output voltage if Vin=15V.

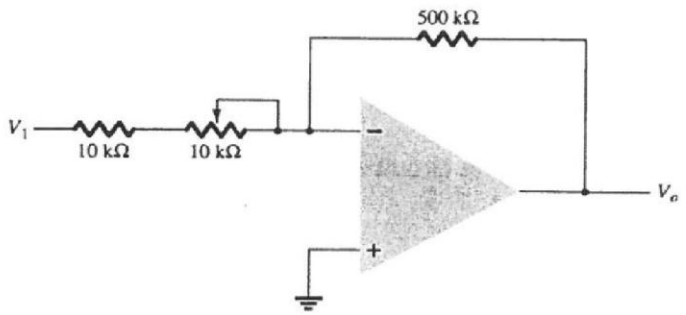

Table Q4(c)

(5 marks)

(c) Based on the equation below,

$$F = (\overline{C + D}) + \bar{A}C\bar{D} + A\bar{B}\bar{C} + \bar{A}\bar{B}CD + AC\bar{D}$$

i. Draw the logic diagram. (4 marks)

ii. Obtain the minimal expressions using Karnaugh Map. (6 marks)

iii. Draw the logic diagram based on Q4(c)(ii) answer. (3 marks)

Question 5(CLO 1 & CLO 2)

(a) Draw the timing diagram for V and Z based Figure Q5 (a)(i). Copy back Figure Q5 (a)(ii) in your answer scheme.

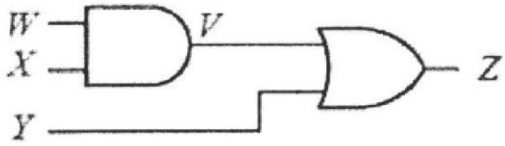

Figure Q5 (a)(i)

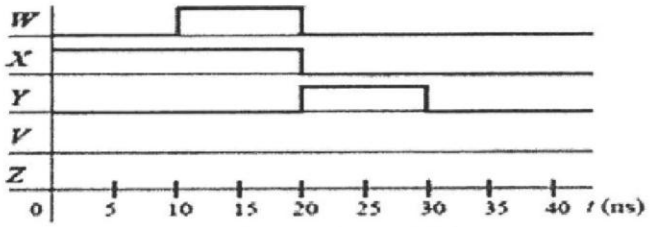

Figure Q5 (a)(ii)

(2 marks)

(b) Determine Ic and V_{EC} for the circuit shown in Figure 5(b).

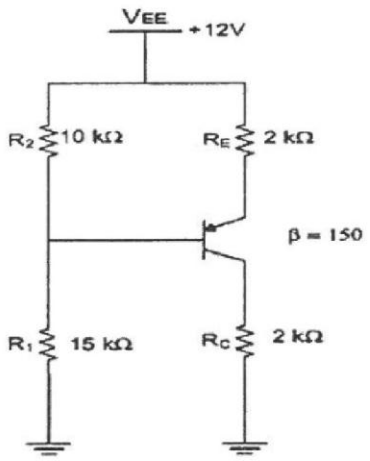

Figure 5(b)

(10 marks)

(c) Based on Figure Q5(c),

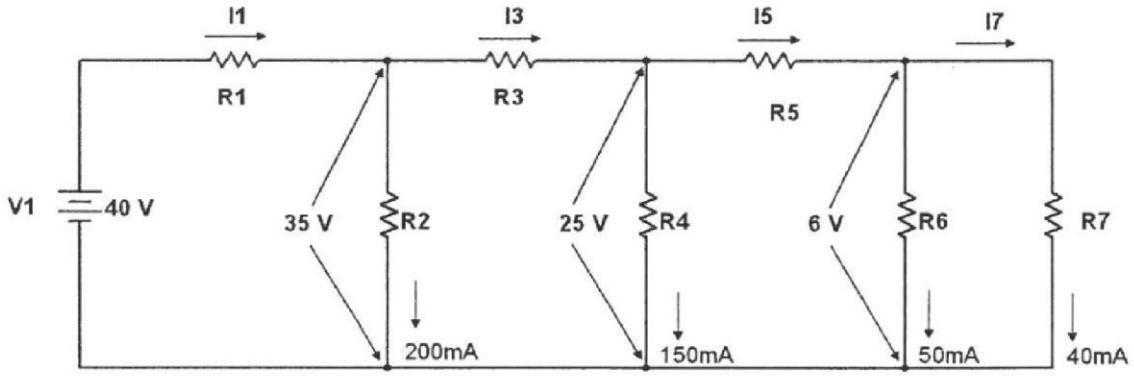

Figure Q5(c)

i. Determine the current I_1, I_3 and I_5.

(5 marks)

ii. Calculate R1, R3, R5 and R7.

(8 marks)

END OF EXAMINATION PAPER