

# UNIVERSITI KUALA LUMPUR MALAYSIAN INSTITUTE OF MARINE ENGINEERING TECHNOLOGY

## FINAL EXAMINATION JANUARY 2016 SEMESTER

**COURSE CODE** 

: LED 20203

**COURSE NAME** 

: DIGITAL ELECTRONICS

PROGRAMME NAME

: DIPLOMA

DATE

: 19 MAY 2016

TIME

: 2.00 PM

DURATION

: 3 HOURS

### **INSTRUCTIONS TO CANDIDATES**

- 1. Please read the instructions given in the question paper CAREFULLY.
- 2. This question paper is printed on both sides of the paper.
- 3. Please write your answers on the answer booklet provided.
- 4. Answer should be written in blue or black ink except for sketching, graphic and illustration.
- 5. This question paper consists of ONE (1) section. Answer FOUR (4) questions only
- 6. Answer all questions in English.

THERE ARE 13 PAGES OF QUESTIONS, INCLUDING THIS PAGE.

SECTION A (Total: 60 marks)

INSTRUCTION: Answer ALL questions.
Please use the answer booklet provided.

#### **Question 1**

a) The numbers given below is represented in BCD numbers. Determine the following questions.

Hint: Use Appendix 1 for ASCII code.

01100110

01111001

000100010001

01110110

i) Convert the message into decimal numbers.

(4 marks)

ii) Convert the message into octal numbers.

(4 marks)

iii) Decode the message into ASCII Code.

(4 marks)

b) Table 1 shows the 8 bits sign numbers for 1's and 2's complement. Determine and rewrite Table 1 in your answer booklet.

Decimal	Magnitude (Binary 8 bits)	1's complement	2's complement
-12			
-30			
+8			
+4			

(8 marks)

### Question 2

- a) Figure 2 shows the combination of logic gates. Answer the following questions.
  - i) Determine the Boolean Expression of output, M.

(5 marks)

ii) Simplify the Boolean Expression by using Boolean Algebra and De'Morgan Theorem.

(3 marks)

iii) Sketch the simplify logic gates in b(ii).

(1 marks)

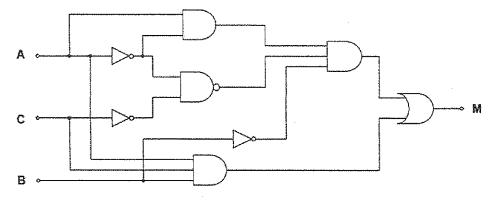


Figure 2: Combination of Logic Gates

- b) Given function  $K = (\overline{M} + \overline{O})(O + \overline{P})$ .
  - i) Construct the Truth Table.

(6 marks)

ii) Simplify your answer in b(i) by using Karnaugh Maps.

(3 marks)

iii) Express the K function, in sum-of-products (SOP) form.

(2 marks)

### Question 3

a) Table 3 presents the comparator controller of sensor liquid tank operation. The sensor has 4 input compartments, A<sub>1</sub>, A<sub>0</sub>, B<sub>1</sub> and B<sub>0</sub>. The output, K can be either in **HIGH** or **LOW** condition. The output of the sensor, K will be **HIGH** only if **A** > **B**.

Table 3: Sensor Liquid Comparator Operation

A <sub>1</sub>	Aο	B <sub>1</sub>	В₀	K
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	-
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

i) Complete the Truth Table in Table 3.

(4 marks)

ii) Determine the Boolean Expression of output, K.

(3 marks)

iii) Simplify the Boolean Expression by using Karnaugh Maps.

(4 marks)

b) Figure 3 shows the 8:1 multiplexer with lo until 17 inputs and 3 selectors, So, S1, and S2.

i) Determine the Boolean Expression of output F in SOP form

(6 marks)

ii) Simplify this expression by using Karnaugh Maps

(3 marks)

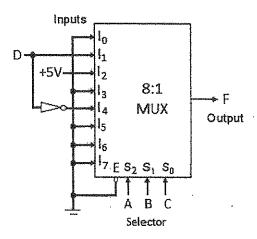


Figure 3: 8:1 Multiplexer

SECTION B (Total: 40 marks)

INSTRUCTION: Answer ALL questions.

Please use the answer booklet provided.

## Question 4

a) Differentiate between an active HIGH of J-K flip-flop and an active LOW S-R Latch in its basic operation? Your answer must include the logic diagram and truth table.

(4 marks)

b) Figure 4a shows the active LOW S-R Latch. Assume that output Q is initially LOW. Draw the waveform that will be observed on the Q and  $\overline{Q}$  output by referring the input signal in Figure 4b. Use Appendix 2 to sketch the outputs.

(4 marks)

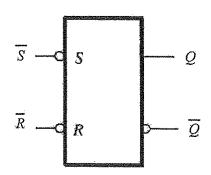


Figure 4a: Active LOW S-R Latch

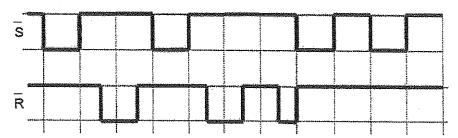


Figure 4b: Input signal for LOW S-R Latch

c) Figure 4c shows the J-K Flip Flop with active HIGH input signal and positive edgetriggered. It can generate two clock waveforms, namely CLK A and CLK B that have an alternating occurrence of pulses. Each waveform is produced by the clock pulse as shown in Figure 4c. Use Appendix 3 to sketch the outputs.

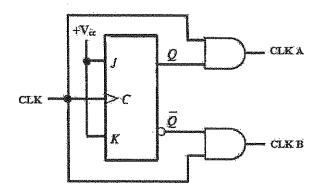
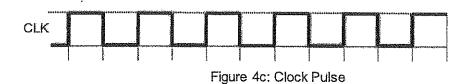


Figure 4c: J-K Flip Flop



i) Sketch the output waveform for J and K.

(2 marks)

ii) Draw the output waveform for Q and  $\overline{Q}$ .

- (4 marks)
- iii) Draw the output waveform for CLK A and CLK B.
- (6 marks)

### Question 5

A Modulus-8 synchronous up-counter is use to count up 8 numbers, which starts from  $0_{10}$  (000<sub>2</sub>) to  $7_{10}$  (111<sub>2</sub>) and count back to  $0_{10}$  (000<sub>2</sub>). Consider the positive edge-triggered of D flip-flops. Answer the following questions:

i) Sketch the State Diagram.

(2 marks)

ii) Construct the State Table.

(4 marks)

iii) State the Transition Table of D flip flops.

(4 marks)

iv) Simplify the expression for each flip-flop using Karnaugh-Maps.

(6 marks)

v) Draw the complete circuit for a Modulus-8 synchronous up-counter.

(4 marks)

#### Question 6

a) A circuit for 4-bit asynchronous binary counter is shown in Figure 6a. Each J-K flip-flop is negative edge-triggered. This asynchronous counter that can be implemented having a modulus-13 with a straight binary sequence from 0000 through 1100. As an engineer, you are required to design an asynchronous counter by determine the following questions:

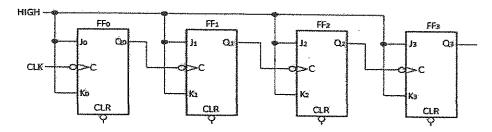


Figure 6a: 4-bit asynchronous binary counter

 Based on block diagram in Figure 6a, draw the complete line connection of 4bit asynchronous binary counter.

(3 marks)

ii) Construct the State Table for each sequence.

(4 marks)

iii) From your answer in (i), draw the logic gate that represents the glitch conditions.

(3 marks)

b) Figure 6b shows the 5-bit register for the specified data input and clock waveforms. Assume that the register is initially cleared (all 0s). Sketch the data states of this register. Use Appendix 4 to sketch the data states.

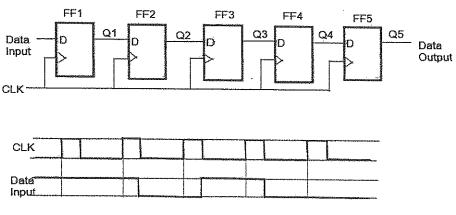


Figure 6b:5-bit register

(10marks)

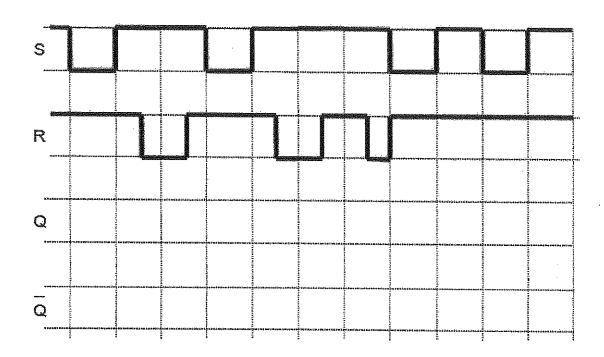
Appendix 1: ASCII Code

1 2 3 4 5 6 7 8 9 9 10 11 12 13 14 14 14 14 16 17	SON STIX ETX EOT ACK BEL BS TES TES TES	(mult) (start of heading) (start of text) (end of text) (end of transmission) (enquiry) (acknowledge) (bell) (backspace) (horizontal tab) (We line feed, new line) (vertical tab)	32 33 34 35 36 37 38 39 40 41	4833; 4834; 4835; 4836; 4837; 4838; 4839;	林 養養養 事。	65 66 67 68 69	4864; 4866; 4866; 4869; 4869; 4870;	森岩正古里下	96 97 98 99 100 101	4#96: 4#97: 5 4#98: b 4#99: c 4#100: d
2 3 4 5 5 6 7 8 9 9 10 111 12 13 14 5 16 6 17	TIX ETX ENQ ENQ EACK BE ES TAB LT YT IF	(stert of text) (end of text) (end of transmission) (enquity) (acknowledge) (beil) (beil) (backspace) (horizontal tah) (Wi line feed, new line)	34 35 36 37 38 39 40 41	4834; 4835; 4836; 4837; 4838; 4839; 4840;	林 養養養 事。	66 67 68 69 70	6866: 6867: 6868; 6869; 6870;	忠主由足下	98 99 100 101	6498; b 6499; c 64100; d
3 4 5 5 5 7 8 9 9 10 11 12 13 14 15 16 6 17	ETX EGT END ACK BEL BS TAB LT YT FF	end of text) (end of transmission) (enquiry) (acknowledge) (belt) (backspace) (horizontal tab) (NI line feed, new line)	35 36 37 38 39 40 41	4333; 4336; 4937; 4438; 4439;	· · · · · · · · · · · · · · · · · · ·	67 68 69 70	6867; 6868; 6869; 6870;	E D E	99 100 101	6#100; 6 6#100; 6
4 5 6 7 8 9 10 11 12 13 14 15 16 17	END ACK BEL BS TAB LF VT	(end of transmission) (enquiry) (acknowledge) (bell) (bels) (backspace) (horizontal tab) (No line feed, new line)	36 37 36 39 40	4#36; 4#37; 4#38; 4#39;	**	68 69 70	6#68; 6#69; 6#70;	D E	100 101	6#100; d 6#101; c
5 6 7 8 9 10 11 12 13 14 14 15	ENQ ACK BEL BS TAB LT VT FF	(enquiry) (acknowledge) (bell) (backspace) (horizontal tab) (Wi line feed, new line)	37 36 39 40 41	4937; 4938; 4939; 4940;	*	69 70	6869; 6870;	E	101	69101; 2
6 7 8 9 10 11 12 13 14 14 16	ACK BEL BS TAB LF VT FF	(acknowledge) (bell) (backspace) (horizontal tam) (WL line Seed, new line)	36 39 40 41	4438; 4439; 4440;	*	70	6#70;	Ŧ		
7 8 9 10 11 12 13 14 15 16	BEL BS TAB LF VT VT	(bell) (backspace) (borizontal tab) (BL line feed, new line)	39 40 41	4#39; 4#40;	å.				102	
8 9 10 11 12 13 14 15	BS TAB LF VT FF	(backspace) (borizontal tab) (BL line feed, new line)	40 41	4440;						≈#102; £
9 10 11 12 13 14 15	TAB LF VT FF	(horizontal tab) (%L line feed, new line)	41			71	487.	G	103	<i>es</i> 103: <i>v</i>
10 11 12 13 14 15 16	LF VT FF	(ML line feed, new line)		- W W -		72	68723	群	104	6\$104; n
11 12 13 14 15 16	vi Pp		A"	441;	)	73	473;	I	105	a#105; i
12 13 14 15 16	FF	(vertical tab)	***	6#4Z:		74	6674:	4	106	4\$106; j
13 14 15 16			43	£#43:		75	4#75:	1	107	69107; k
14 15 16 17	CR	(NP form feed, new page)	44	44 44 t		76	4576;	L	108	€\$108: 1
15 16 17		(corriege return)	45	6#45:	*	77	£#775	M	103	£\$109; w
16 17		(shaft out)	46	49 96 :		78	4#785	N	110	asild: n
17	21	(shift in)	47	6847;	1	79	48795	0	111	esill: 0
		(data link escape)	48	6446;	0	80	¢\$\$0;	₽.	112	65112; p
	DCI	(device control 1)	49	449:	1	81	<b>表现</b> 。	10	113	4#113; q
	DC2	(device control 2)	50	G#50;	2	82	4482:	30	114	6\$114: T
	DC3	(device control 3)	51	C#51;	3	83	6#83;	3	113	€\$115; #
	TYC4	(device control 4)	52	6#52:		84	4#84;	T	116	sfile: t
	NAK -	(negative soknowledge)	253	4453;	-5	85	4665	U	117	4#117; u
	SYN	(synchronous idle)	54	C#54:	· 6	86	6#86;	7/	116	€£118; ¥
	LIB.	(end of trens. block)	\$5	4#55;	7	87	点棒87;	N/	119	65119; W
	TAN	(cencel)	56	6256;	8	88	4#80;	1.	120	€\$120; ×
	X.H.	(end of medicin)	57	6357;	\$	89	4#89;	Y	121	€\$121; y
		(substitute)	58	: 52%2		90	G\$90;	芝.	122	4\$122; E
	ESC	(cacupe)	59	6459:	2	91	K#91:	Ť	123	6\$123; f
		(file separator)	60	¢#60:		92	6 <b>492</b> ;		124	c#124;
		(group separator)	<b>61</b>	6961;		93	æ#93;	3	125	6#125; }
		(record separator)	62	4062:	>	94	6/9/1;	÷	126	4\$125: -
31	US	(unit separator)	63	66633	7	95	6#95:		127	ε\$127; DE

Appendix 2: (Question 4b)

Name: ID No:

Table No:



Appendix 3 (Question 4c)

Name: ID No: Table No:

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Appendix 4 (Question 6b)

Name: ID No: Table No:

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_											······································	
Q2							<del></del>	,		~~~		
_			 ***						***************************************			
Q3				····								
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Q4	· · · .		 				***************************************					
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Q5												