UNIVERSITI KUALA LUMPUR
MALAYSIAN INSTITUTE OF MARINE ENGINEERING TECHNOLOGY

FINAL EXAMINATION
JANUARY 2016 SEMESTER

COURSE CODE	:	LED 20203
COURSE NAME	:	DIGITAL ELECTRONICS
PROGRAMME NAME	:	DIPLOMA
DATE	:	19 MAY 2016
TIME	:	2.00 PM
DURATION	:	3 HOURS

INSTRUCTIONS TO CANDIDATES

1. Please read the instructions given in the question paper CAREFULLY.
2. This question paper is printed on both sides of the paper.
3. Please write your answers on the answer booklet provided.
4. Answer should be written in blue or black ink except for sketching, graphic and illustration.
5. This question paper consists of ONE (1) section. Answer FOUR (4) questions only
6. Answer all questions in English.

THERE ARE 13 PAGES OF QUESTIONS, INCLUDING THIS PAGE.

SECTION A (Total: 60 marks)

INSTRUCTION: Answer ALL questions.
Please use the answer booklet provided.

Question 1

a) The numbers given below is represented in BCD numbers. Determine the following questions.

Hint: Use Appendix 1 for ASCII code.

01100110 01111001 000100010001 01110110

i) Convert the message into decimal numbers.

(4 marks)

ii) Convert the message into octal numbers.

(4 marks)

iii) Decode the message into ASCII Code.

(4 marks)

b) Table 1 shows the 8 bits sign numbers for 1's and 2's complement. Determine and rewrite Table 1 in your answer booklet.

Decimal	Magnitude (Binary 8 bits)	1's complement	2's complement
-12			
-30			
+8			
+4			

(8 marks)

Question 2

a) Figure 2 shows the combination of logic gates. Answer the following questions.

i) Determine the Boolean Expression of output, M.

(5 marks)

ii) Simplify the Boolean Expression by using Boolean Algebra and De'Morgan Theorem.

(3 marks)

iii) Sketch the simplify logic gates in b(ii).

(1 marks)

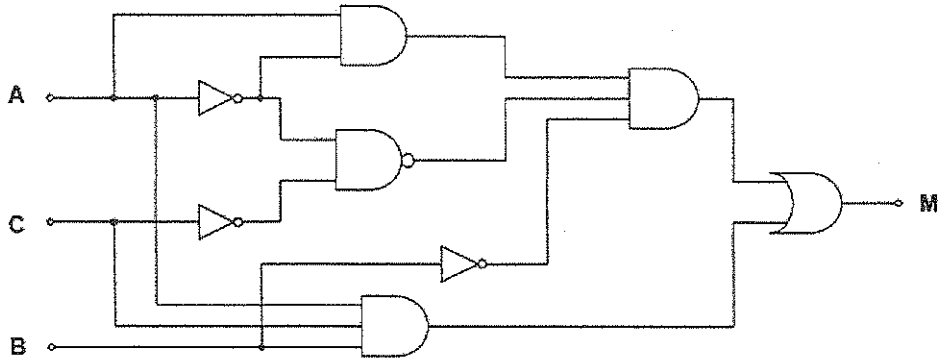


Figure 2: Combination of Logic Gates

b) Given function $K = (\overline{M} + \overline{O})(O + \overline{P})$.

i) Construct the Truth Table.

(6 marks)

ii) Simplify your answer in b(i) by using Karnaugh Maps.

(3 marks)

iii) Express the *K* function, in sum-of-products (SOP) form.

(2 marks)

Question 3

a) Table 3 presents the comparator controller of sensor liquid tank operation. The sensor has 4 input compartments, A_1, A_0, B_1 and B_0. The output, K can be either in **HIGH** or **LOW** condition. The output of the sensor, K will be **HIGH** only if **A > B.**

Table 3: Sensor Liquid Comparator Operation

A_1	A_0	B_1	B_0	K
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

i) Complete the Truth Table in Table 3.

(4 marks)

ii) Determine the Boolean Expression of output, K.

(3 marks)

iii) Simplify the Boolean Expression by using Karnaugh Maps.

(4 marks)

b) Figure 3 shows the 8:1 multiplexer with I_0 until I_7 inputs and 3 selectors, S_0, S1, and S_2.

i) Determine the Boolean Expression of output F in SOP form

(6 marks)

ii) Simplify this expression by using Karnaugh Maps

(3 marks)

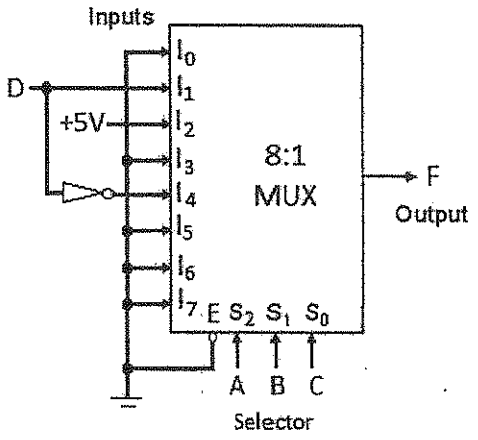


Figure 3: 8:1 Multiplexer

SECTION B (Total: 40 marks)

INSTRUCTION: Answer ALL questions.
Please use the answer booklet provided.

Question 4

a) Differentiate between an active HIGH of J-K flip-flop and an active LOW S-R Latch in its basic operation? Your answer must include the logic diagram and truth table.

(4 marks)

b) Figure 4a shows the active LOW S-R Latch. Assume that output Q is initially LOW. Draw the waveform that will be observed on the Q and $\overline{Q}$ output by referring the input signal in Figure 4b. Use Appendix 2 to sketch the outputs.

(4 marks)

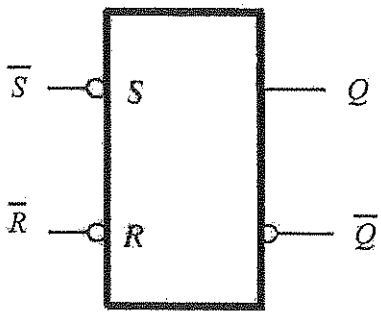


Figure 4a: Active LOW S-R Latch

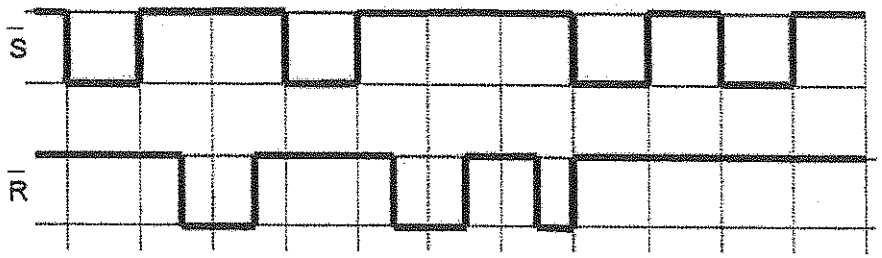


Figure 4b: Input signal for LOW S-R Latch

c) Figure 4c shows the J-K Flip Flop with active HIGH input signal and positive edge-triggered. It can generate two clock waveforms, namely CLK A and CLK B that have an alternating occurrence of pulses. Each waveform is produced by the clock pulse as shown in Figure 4c. Use Appendix 3 to sketch the outputs.

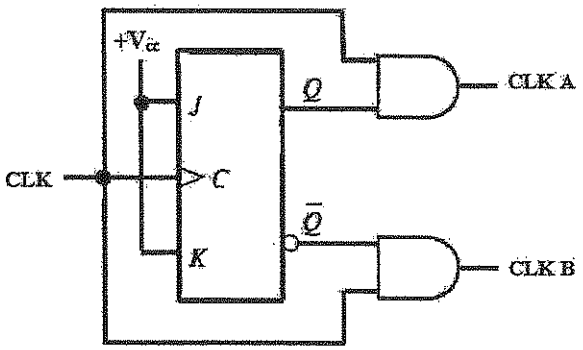


Figure 4c: J-K Flip Flop

Figure 4c: Clock Pulse

i) Sketch the output waveform for J and K.

(2 marks)

ii) Draw the output waveform for Q and $\overline{Q}$.

(4 marks)

iii) Draw the output waveform for CLK A and CLK B.

(6 marks)

Question 5

A Modulus-8 synchronous up-counter is use to count up 8 numbers, which starts from 0_{10} (000_2) to 7_{10} (111_2) and count back to 0_{10} (000_2). Consider the positive edge-triggered of D flip-flops. Answer the following questions:

i) Sketch the State Diagram.

(2 marks)

ii) Construct the State Table.

(4 marks)

iii) State the Transition Table of D flip flops.

(4 marks)

iv) Simplify the expression for each flip-flop using Karnaugh-Maps.

(6 marks)

v) Draw the complete circuit for a Modulus-8 synchronous up-counter.

(4 marks)

Question 6

a) A circuit for 4-bit asynchronous binary counter is shown in Figure 6a. Each J-K flip-flop is negative edge-triggered. This asynchronous counter that can be implemented having a modulus-13 with a straight binary sequence from 0000 through 1100. As an engineer, you are required to design an asynchronous counter by determine the following questions:

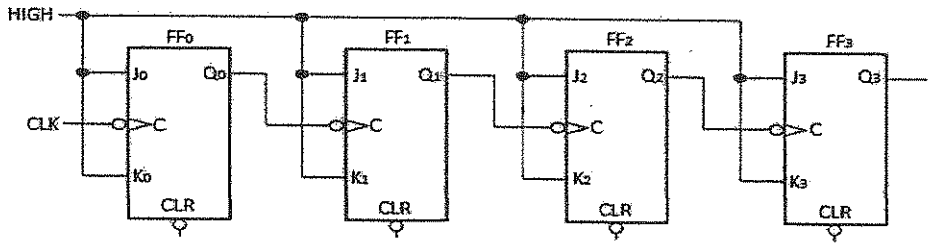


Figure 6a: 4-bit asynchronous binary counter

i) Based on block diagram in Figure 6a, draw the complete line connection of 4-bit asynchronous binary counter.

(3 marks)

ii) Construct the State Table for each sequence.

(4 marks)

iii) From your answer in (i), draw the logic gate that represents the glitch conditions.

(3 marks)

b) Figure 6b shows the 5-bit register for the specified data input and clock waveforms. Assume that the register is initially cleared (all 0s). Sketch the data states of this register. Use Appendix 4 to sketch the data states.

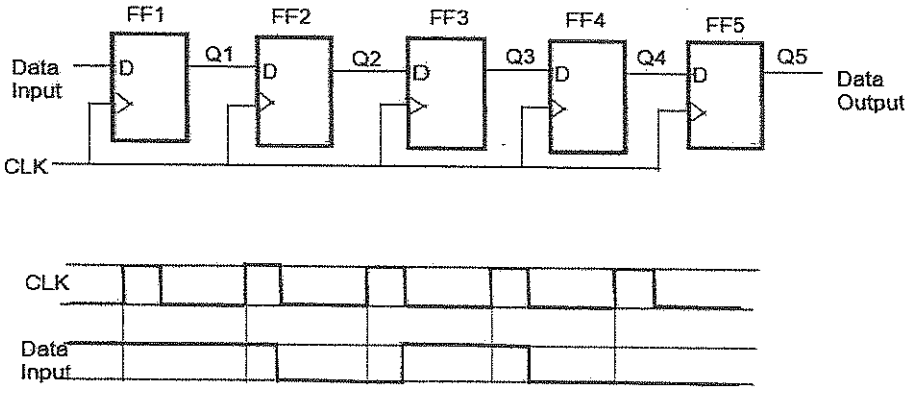


Figure 6b:5-bit register

(10marks)

Appendix 1:

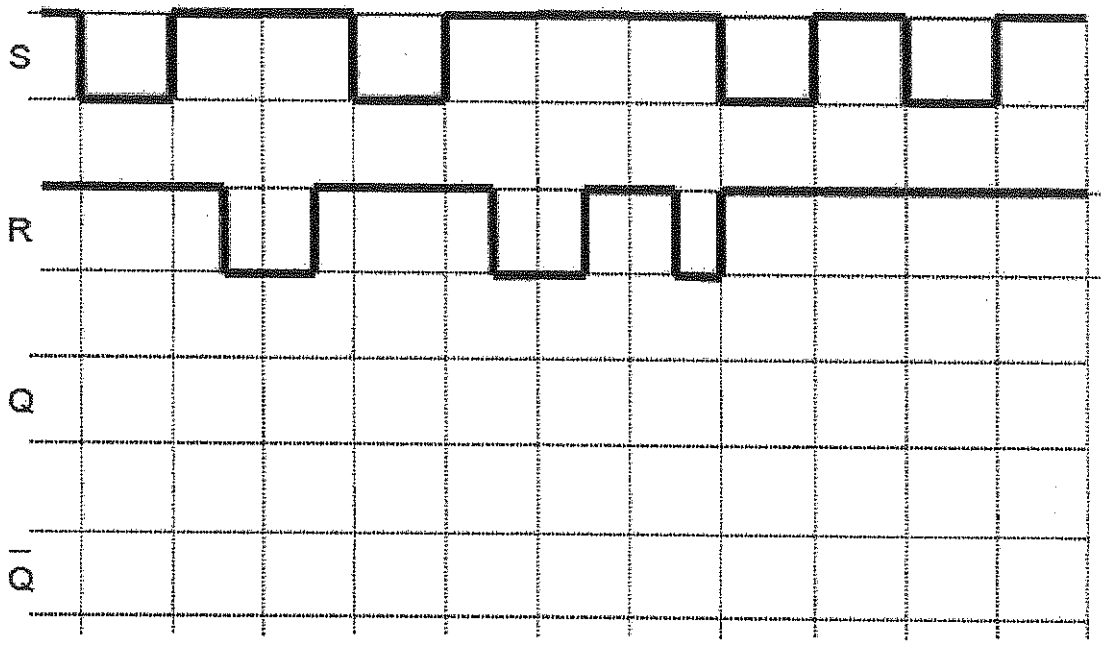
ASCII Code

Dec	Hx	Oct	Char	Dec	Hx	Oct	Html	Chr	Dec	Hx	Oct	Html	Chr	Dec	Hx	Oct	Html	Chr
0			NUL (null)	32				Space	64			@	@	96			`	`
1			SOH (start of heading)	33			!	!	65			A	A	97			a	a
2			STX (start of text)	34			"	"	66			B	B	98			b	b
3			ETX (end of text)	35			#	#	67			C	C	99			c	c
4			EOT (end of transmission)	36			$	$	68			D	D	100			d	d
5			ENQ (enquiry)	37			%	%	69			E	E	101			e	e
6			ACK (acknowledge)	38			&	&	70			F	F	102			f	f
7			BEL (bell)	39			'	'	71			G	G	103			g	g
8			BS (backspace)	40			(	(	72			H	H	104			h	h
9			TAB (horizontal tab)	41			)	)	73			I	I	105			i	i
10			LF (NL line feed, new line)	42			*	*	74			J	J	106			j	j
11			VT (vertical tab)	43			+	+	75			K	K	107			k	k
12			FF (NP form feed, new page)	44			,	,	76			L	L	108			l	l
13			CR (carriage return)	45			-	-	77			M	M	109			m	m
14			SO (shift out)	46			.	.	78			N	N	110			n	n
15			SI (shift in)	47			/	/	79			O	O	111			o	o
16			DLE (data link escape)	48			0	0	80			P	P	112			p	p
17			DC1 (device control 1)	49			1	1	81			Q	Q	113			q	q
18			DC2 (device control 2)	50			2	2	82			R	R	114			r	r
19			DC3 (device control 3)	51			3	3	83			S	S	115			s	s
20			DC4 (device control 4)	52			4	4	84			T	T	116			t	t
21			NAK (negative acknowledge)	53			5	5	85			U	U	117			u	u
22			SYN (synchronous idle)	54			6	6	86			V	V	118			v	v
23			ETB (end of trans. block)	55			7	7	87			W	W	119			w	w
24			CAN (cancel)	56			8	8	88			X	X	120			x	x
25			EM (end of medium)	57			9	9	89			Y	Y	121			y	y
26			SUB (substitute)	58			:	:	90			Z	Z	122			z	z
27			ESC (escape)	59			;	;	91			[	[	123			{	{
28			FS (file separator)	60			<	<	92			\	\	124					|
29			GS (group separator)	61			=	=	93			]	]	125			}	}
30			RS (record separator)	62			>	>	94			^	^	126			~	~
31			US (unit separator)	63			?	?	95			_	_	127			&#127;	DEL

Source: www.LookupTables.com

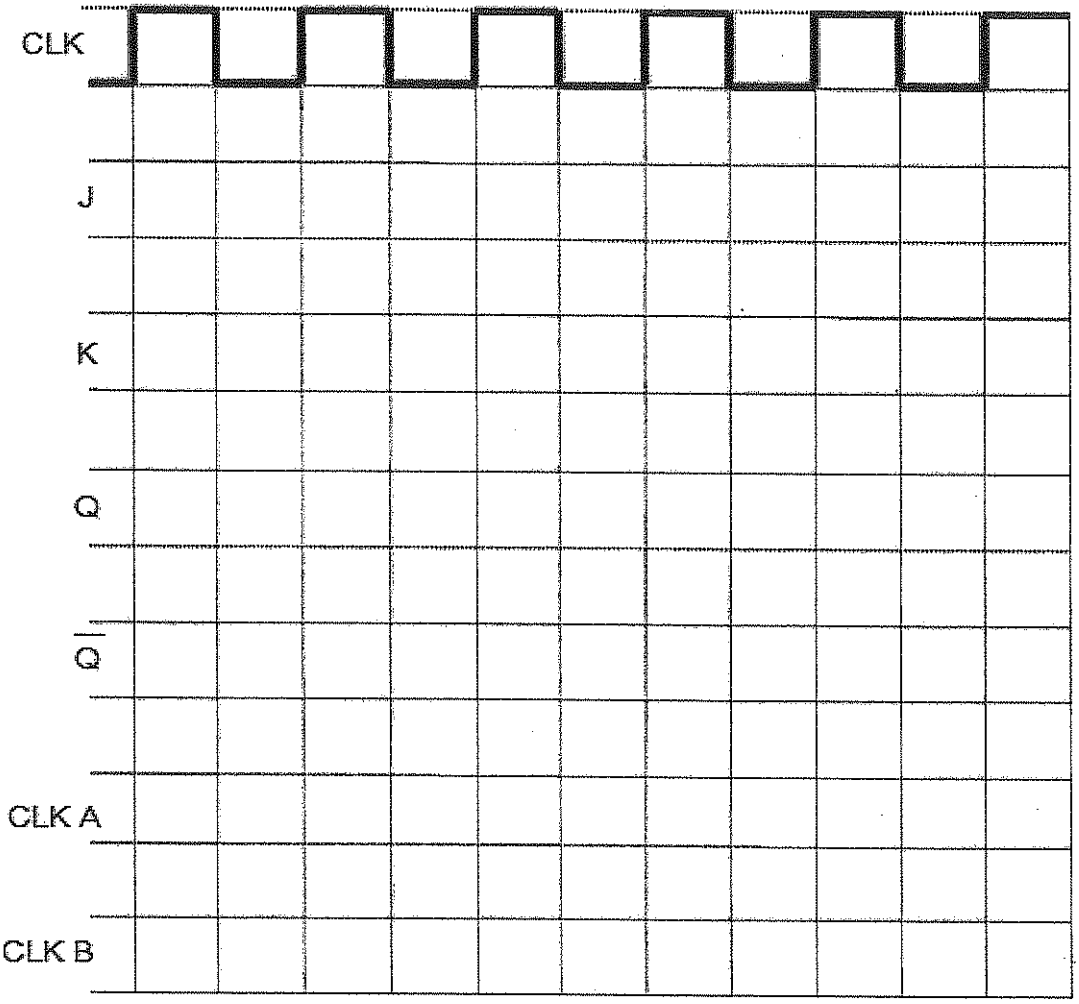
Appendix 2:
(Question 4b)

Name:
ID No:
Table No:



Appendix 3
(Question 4c)

Name:
ID No:
Table No:



Appendix 4

(Question 6b)

Name:

ID No:

Table No: