UNIVERSITI KUALA LUMPUR
MALAYSIAN INSTITUTE OF INDUSTRIAL TECHNOLOGY

FINAL EXAMINATION

JANUARY 2016 SEMESTER

COURSE CODE	:	JCB 10503
COURSE TITLE	:	ANALOG ELECTRONICS
PROGRAMME LEVEL	:	BACHELOR
DATE	:	30 MAY 2016
TIME	:	9.00 AM – 12.00 PM
DURATION	:	3 HOURS

INSTRUCTIONS TO CANDIDATES

1. Please read the instructions given in the question paper CAREFULLY.
2. This question paper is printed on both sides of the paper.
3. This question paper consists of ONE (1) section.
4. Answer FIVE (5) questions ONLY in Section A.
5. Please write your answers on the answer booklet provided.
6. Please answer all questions in English only.

THERE ARE 7 PAGES OF QUESTIONS EXCLUDING THIS PAGE.

SECTION A (Total: 100 marks)

INSTRUCTION: Answer FIVE (5) questions ONLY.
Please use the answer booklet provided.

Question 1

(a) With the aid of suitable diagram, discuss **TWO (2)** characteristics of conductor and insulator.

(6 marks)

(b) A 2V stabilized power supply is required to be produced from a 20V DC power supply input source. The maximum power rating, P_Z of the zener diode is 2.3W. Using the following zener regulator circuit, solve:

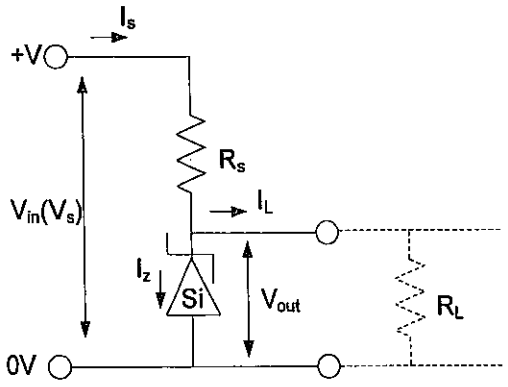


Figure 1: Zener regulator circuit.

(i) The maximum current flowing through the zener diode.

(2 marks)

(ii) The minimum value of the series resistor, R_S.

(2 marks)

(iii) The load current I_L if a load resistor of 1kΩ is connected across the zener diode.

(2 marks)

(iv) The zener current I_Z at full load.

(2 marks)

(c) Examine the input and output waveform of a rectifier circuit as shown in Figure 2. Classify the type of the rectifier. Then, design the required rectifier circuit using ideal diodes.

(6 marks)

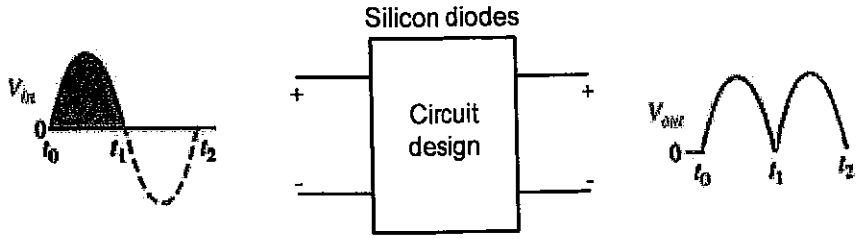


Figure 2: Input and output waveform of rectifier circuit.

Question 2

(a) With the aid of suitable diagram, differentiate **TWO (2)** characteristics between common base and common emitter configurations.

(6 marks)

(b) From Figure 3, prove that the base current, $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ and collector-to-emitter voltage, $V_{CE} = V_{CC} - I_C R_C$. Illustrate the input and output loop circuit.

(6 marks)

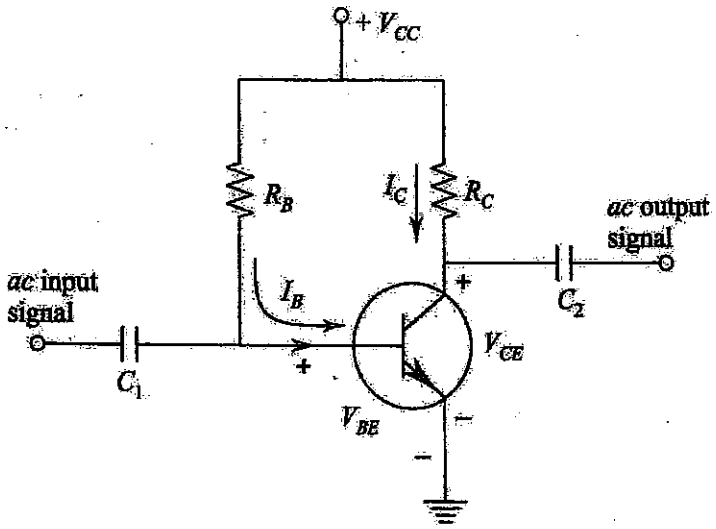


Figure 3: Fixed-bias circuit of a transistor.

(c) Using the same fixed-bias circuit in part b and given the values of $V_{CC} = 25V, R_B = 205k\Omega, R_C = 1.2k\Omega, \beta = 100$, determine:

(i) Base current, I_B.

(2 marks)

(ii) Collector current, I_C.

(2 marks)

(iii) Collector-to-emitter voltage, V_{CE}.

(2 marks)

(iv) Base voltage, V_B.

(2 marks)

Question 3

(a) Compare **FOUR (4)** characteristics of bipolar junction transistor (BJT) and filed-effect transistor (FET).

(4 marks)

(b) Given the value of maximum drain saturation current, $I_{DSS} = 5\,mA$ and peak voltage, $V_P = -4\,V$. For the self-bias configuration of Figure 4, determine:

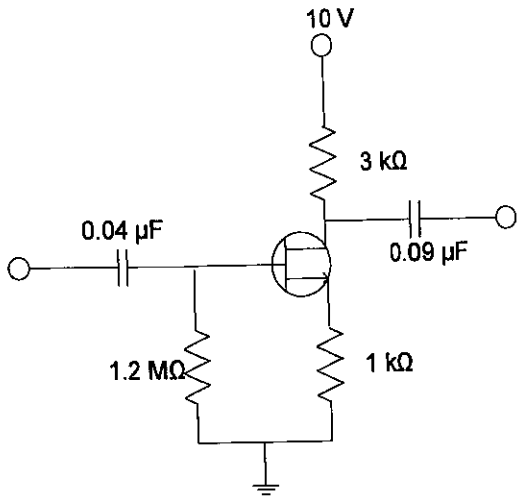


Figure 4: Self bias configuration circuit.

(i) Gate to source voltage, V_{GSQ}.

(8 marks)

(ii) Drain current, I_{DQ}.

(1 mark)

(iii) Drain to source voltage, V_{DS}.

(2 marks)

(iv) Source voltage, V_S.

(2 marks)

(v) Gate voltage, V_G.

(1 mark)

(vi) Drain voltage, V_D.

(2 marks)

Question 4

(a) Explain **FOUR (4)** characteristics of a good amplifier.

(4 marks)

(b) Figure 5 illustrates the BJT amplifier circuit. Given the parameters of the amplifier is $\beta = 100$, $r_{bb'} = 20\Omega$, $r_{ce} = 20\Omega$ and $V_{BE} = 0.7V$. From the figure,

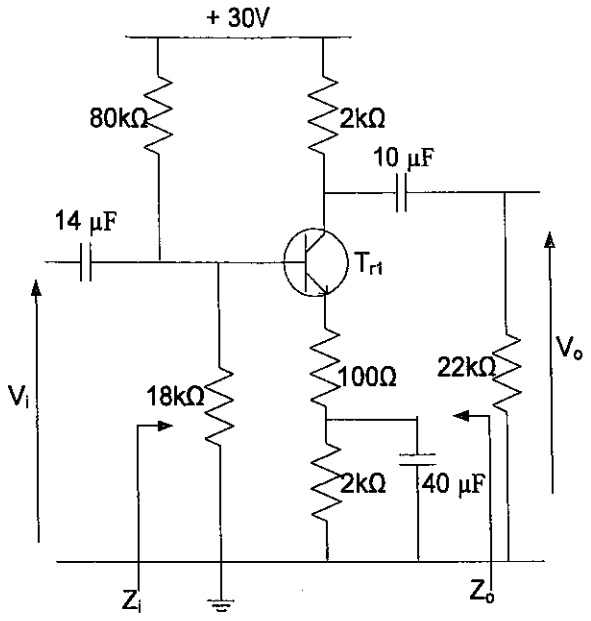


Figure 5: BJT amplifier circuit.

(i) Predict the types of BJT configuration for the amplifier circuit.

(2 marks)

(ii) Design the AC equivalent amplifier circuit using hybrid-π model.

(5 marks)

(iii) Examine emitter current, I_E and r_e.

(5 marks)

(iv) Examine input and output impedances, Z_i and Z_o.

(2 marks)

(v) Examine voltage and current gain, A_v and A_i.

(2 marks)

Question 5

(a) With the aid of suitable diagram, explain a concept of positive and negative feedbacks.

(6 marks)

(b) Figure 6 shows an output of a periodic waveform of a 555 timer. To generate the periodic waveform,

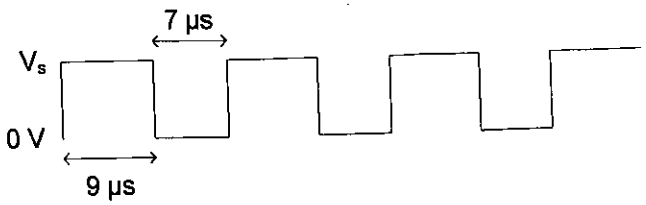


Figure 6: An output of a periodic waveform of 555 timer.

(i) Design a circuit using the 555 timer. Use capacitor values of 0.01 µF. Draw and label the 555 timer.

(6 marks)

(ii) Modify the circuit in part (i) to give a duty cycle of 20% without changing the value of the frequency. Draw and label the modified 555 timer circuit. Then, interpret the operation of the circuit.

(8 marks)

Question 6

(a) Figure 7 illustrates a basic connection of operational amplifier (op-amp) circuit. By applying an ideal op-amp characteristics, design the op-amp AC equivalent circuit. Draw and label the equivalent circuit.

(6 marks)

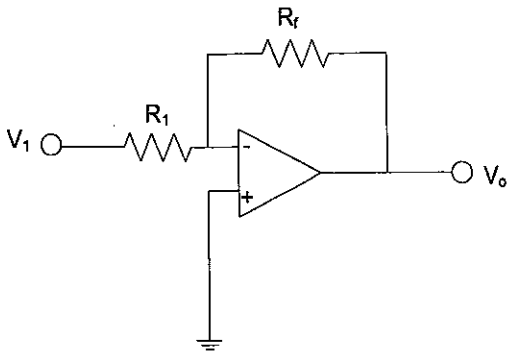
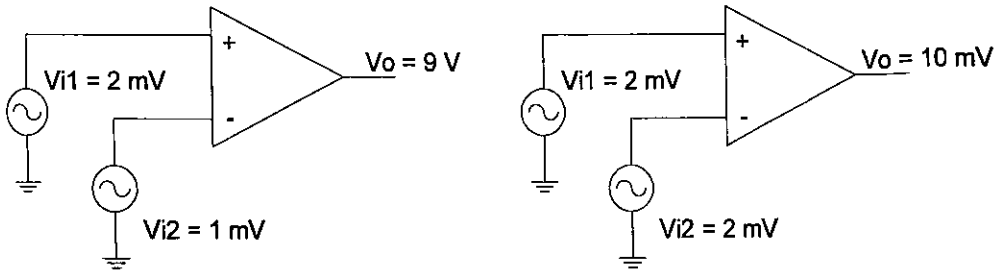


Figure 7: Basic connection of operational amplifier circuit.

(b) Figure 8 shows a differential and common-mode operation for an operational amplifier. Solve:



(a) Differential operation (b) Common-mode operation

Figure 8: Operational amplifier circuits.

(i) Differential input voltage, V_d. Draw the equivalent circuit for the differential operation.

(4 marks)

(ii) Common input voltage, V_c. Draw the equivalent circuit for the common-mode operation.

(4 marks)

(iii) Common-mode rejection ratio, CMRR.

(6 marks)

END OF EXAMINATION PAPER