CONFIDENTIAL

UNIVERSITI KUALA LUMPUR
MALAYSIAN INSTITUTE OF INFORMATION TECHNOLOGY

FINAL EXAMINATION

JANUARY 2016 SEMESTER

SUBJECT CODE	:	IED12303
SUBJECT TITLE	:	DIGITAL ELECTRONICS
LEVEL	:	DIPLOMA
TIME / DURATION	:	(2 ½ HOURS) 9.00 am – 11.30 am
DATE	:	24 MAY 2016

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INSTRUCTIONS TO CANDIDATES

1. Please read the instructions given in the question paper CAREFULLY.
2. This question paper is printed on both sides of the paper.
3. This question paper consists of TWO (2) sections.
4. Answer all questions of Section A, and THREE (3) questions of Section B.
5. Please write your answers on the answer booklet provided.
6. Answer all questions in English.

SECTION A (Total: 25 marks)

INSTRUCTION: Answer ALL questions
Please use the answer booklet provided.

Question 1: Multiple Choice Questions

1. When the input to a inverter is LOW (0), the output is _____ .
   (A) HIGH or 1 (B) LOW or 1 (C) HIGH or 0 (D) LOW or 0

2. A quantity having continuous value is _____ .
   (A) a digital quantity (B) an analog quantity
   (C) a binary quantity (D) a natural quantity

3. The output of an AND gate with inputs A, B, and C is a 1 (HIGH) when _____ .
   (A) A=0, B=0, C=0 (B) A=0, B=1, C=1
   (C) A=1, B=1, C=0 (D) A=1, B=1, C=1

4. A pulse in a certain waveform occurs every 10 ms. The frequency is _____ .
   (A) 1 kHz (B) 1 Hz (C) 100 Hz (D) 10 Hz

5. The complement of a variable is always _____ .
   (A) 0 (B) 1 (C) equal to the variable (D) the inverse of the variable

6. In a certain digital waveform, the period is twice the pulse width. The duty cycle is _____ .
   (A) 100% (B) 200% (C) 50% (D) 33.3%

7. The Boolean expression $W\overline{XY}$ is _____
   (A) a sum term (B) a product term (C) a literal term (D) always 1

8. An example of a data storage device is _____ .
   (A) the AND gate (B) the OR gate
   (C) the flip-flop (D) the comparator

9. According to the commutative law of addition, _____ .
   (A) AB = BA (B) B = B + B
   (C) (A + B) + C = A + (B + C) (D) B + A = A + B

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10. If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be _____ .
    (A) Set (B) reset (C) invalid (D) clear

11. According to the distributive law, _____.
    (A) B(A + C) = AB + BC (B) (AB)C = ABC
    (C) (B + 1)B = B (D) A +AB = A

12. The invalid state of an S-R latch occurs when _____ .
    (A) S=1, R=0 (B) S=0, R=1
    (C) S=1, R=1 (D) S=0, R=0

13. Which of the following rules states that if one input of an AND gate is always 1, the output is equal to the other input? _____
    (A) B · 1 = B (B) B + B = B (C) B · B = B (D) B + 1 = 1

14. For a gated D latch, the Q output always equals the D input _____ .
    (A) before the enable pulse (B) during the enable pulse
    (C) Immediately after the enable pulse (D) answers (B) and (C)

15. The Boolean expression X = ABC + ACD represents _____ .
    (A) an exclusive-OR (B) two ANDs ORed together
    (C) two ORs ANDed together (D) a 4-input AND gate

16. Like the latch, the flip-flop belongs to a category of logic circuits known as _____.
    (A) monostable multivibrators (B) bistable multibrators
    (C) astable multivibrators (D) one-shots

17. An example of a product-of-sums expression is _____ .
    (A) $A(B+C)+A\overline{C}$ (B) $(A+B)(\overline{A}+B+\overline{C})$
    (C) $\overline{A}+\overline{B}+BC$ (D) both answers (A) and (B)

18. The purpose of the clock input to a flip-flop is to _____ .
    (A) clear the device

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(B) set the device

(C) always cause the output to change states

(D) cause the output to assume a state dependent on the controlling (S-R, J-K, or D) inputs

19. An example of a standard SOP expression is _____ .

(A) $A\overline{B}C\overline{D}+\overline{A}B+\overline{A}$ (B) $A\overline{B}C+A\overline{C}D$

(C) $A\overline{B}+\overline{A}B+AB$ (D) $\overline{A}B+A\overline{B}C+AB\overline{D}$

20. A 4-variable Karnaugh map has _____ .

(A) eight cells (B) three cells (C) sixteen cells (D) four cells

21. For an edge-triggered D flip-flop, _____ .

(A) a change in the state of the flip-flop can occur only at a clock pulse edge

(B) the state that the flip-flop goes to depends on the D input

(C) the output follows the input at each clock pulse

(D) all of these answers

22. A feature that distinguishes the J-K flip-flop from the S-R flip-flop is the _____ .

(A) toggle condition (B) preset input

(C) type of clock (D) clear input

23. A flip-flop is in the toggle condition when _____ .

(A) J=1, K=0 (B) J=1, K=1

(C) J=0, K=0 (D) J=0, K=1

24. A J-K flip-flop with J=1 and K=1 has a 10 kHz clock input. The Q output is _____ .

(A) constantly HIGH (B) constantly LOW

(C) a 10 kHz square wave (D) a 5 kHz square wave

25. A 5-variable Karnaugh map has _____ .

(A) 4 cells (B) eight cells (C) sixteen cells (D) none of these

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SECTION B (Total: 75 marks)

INSTRUCTION: Answer any THREE (3) of the FOUR (4) questions
Please use the answer booklet provided.

Question 2

1. A portion of a periodic digital waveform is shown in Figure 1. Determine the following:
   a. period
   b. frequency
   c. duty cycle

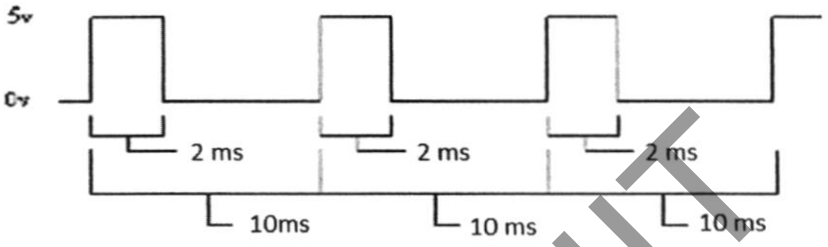

Figure 1

(3 marks)

2. Convert the following decimal values to binary using Divided-by-Two method.
   a. 95
   b. 139

(6 marks)

3. Convert the following decimal values to binary using Sum-of-Weights method.
   a. 96
   b. 140

(6 marks)

4. Express decimal number +27 and -27 as 8-bit numbers in the sign-magnitude, 1's complement, and 2's complement forms.

(6 marks)

5. Convert the decimal number 127 to BCD code. Convert the BCD code 100100000011 to decimal.

(4 marks)

[Total: 25 marks]

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Question 3

Table 1 is the truth table of a circuit with output X and four inputs A, B, C, and D.

Table 1.

INPUTS				OUTPUT
A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

a. Create Karnaugh map according Table 1.

(8 marks)

b. Determine the simplest Boolean expression with the Karnaugh map in question (a).

(9 marks)

c. Implement the Boolean expression of question (B) with AND, OR, and NOT gates.

(8 marks)

[Total: 25 marks]

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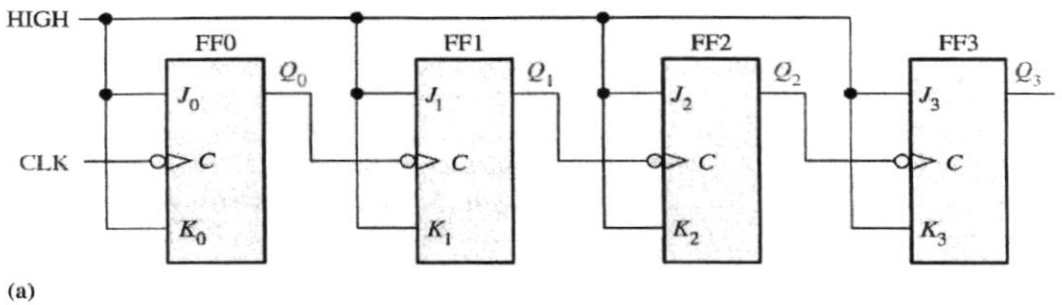
Question 4

A 4-bit binary counter is shown in Figure 2. Each flip-flop has a propagation delay for 10 nanoseconds (ns).



(a)

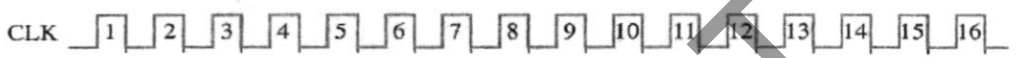


Figure 2

a. Is it a synchronous or asynchronous counter? Justify your answer.

(3 marks)

b. Is it a positive or negative edge-triggered counter?

(2 marks)

c. For clock CLK in Figure 2 applied to the first flip-flop, develop a timing diagram showing the Q output of each flip-flop.

(12 marks)

d. Determine the total propagation delay time from the triggering edge of a clock pulse until a corresponding change can occur in the state of Q_3.

(4 marks)

e. Determine the maximum clock frequency at which the counter can be operated.

(4 marks)

[Total: 25 marks]

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Question 5

1. Using Boolean algebra and DeMorgan's theorems to simply following expressions.
   a. $\overline{\overline{(A+B)}\,\overline{(C+D)}\,\overline{(E+F)}\,\overline{(G+H)}}$

   b. $(B+BC)(B+\overline{B}C)(B+D)$

   c. $A+B[AC+(B+\overline{C})D]$

(9 marks)

2. Develop a truth table for each of the SOP (Sum of Products) expression:
   a. $\overline{A}B\overline{C}D+A\overline{B}C\overline{D}+A\overline{B}CD+\overline{A}BC\overline{D}$

   b. $\overline{X}+Y\overline{Z}+WZ+X\overline{Y}Z$

(8 marks)

3. For each truth table in Figure 3, derive a standard SOP (Sum-of-Products) expression.

A B C	X
0 0 0	0
0 0 1	0
0 1 0	0
0 1 1	0
1 0 0	0
1 0 1	1
1 1 0	1
1 1 1	1

A B C D	X
0 0 0 0	1
0 0 0 1	1
0 0 1 0	0
0 0 1 1	1
0 1 0 0	0
0 1 0 1	1
0 1 1 0	1
0 1 1 1	0
1 0 0 0	0
1 0 0 1	1
1 0 1 0	0
1 0 1 1	0
1 1 0 0	1
1 1 0 1	0
1 1 1 0	0
1 1 1 1	0

.,Figure 3

(8 marks)

[Total: 25 marks]

END OF QUESTIONS

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